Acid Copper Plating Process for IC Substrate Applications

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ABSTRACT

Two challenges that advanced packaging suppliers are faced with during IC substrate fabrication are meeting the copper plating performance requirements and reducing manufacturing process costs. The copper plating must provide both high resolution and strict height uniformity within unit (WIU) and within a die/panel (WID). Plated features, such as fine lines and pillars, whose top shape and coplanarity are critical to the product quality. A non-planar surface could result in signal transmission loss and introduce weak points in the connections. Therefore, copper plating solutions providing uniform, planar structures, that don't require any special post treatment are highly desirable features for both redistribution layer (RDL) and pillar plating processes. The copper plating solution can also reduce cost by plating two or three types of features in a single step or from a single process bath. This flexibility allows fabricators to save on space and equipment.

In this paper, an electroplating (EP) package is introduced to plate both RDL and pillars under different current densities in vertical continuous platers (VCP). The plating uniformity and coplanarity of both RDL fine lines and pillars was evaluated on a panel level.

The EP package offered excellent coplanarity within a pattern unit for RDL plating. The variation in the plated height (or thickness) between fine lines and pads, of 5 and 50 µm widths respectively, was below 1.0 µm when using a current density of 1.5 A/dm^2 (ASD) for 66 minutes. For 10 µm wide lines, the plated copper thickness variation can be below 0.5 µm. The variation of plated thickness across 410 mm x 510 mm panels was below 1.0 µm, when the plated panel was measured at 3 points (top, middle, and bottom). The tops of the fine lines have defined, rectangular shapes. These types of profiles have excellent conductivity.

For pillar plating under higher current density, such as 5-10 ASD, the top of the pillars had slightly domed profiles. The pillars were very uniform within the die and within the panel.

Physical properties of the plated copper deposit are essential for the reliability of the finished product. A few key physical properties are tensile strength, elongation %, and internal stress. These properties show the tolerance of the deposit for thermal stress and warpage. The additives (wetter, leveler, and brightener) strongly influence the physical properties of the deposit. Copper deposited with the EP package has tensile strength above 40,000 psi, elongation % above 18%, and internal stress below 1.0 Kg/mm^2. The physical properties of the deposited copper did not change considerably during bath aging, showing that the package has stable performance.

The reliability of both pillars and RDL features were evaluated via solder dip. The RDL features were dipped at 288°C, 6 times. The pillars were dipped at 288°C, 60 times. Neither feature showed any cracks or separation from the substrate.

INTRODUCTION

Panel-Level Packaging (PLP) is gradually being adopted to meet the packaging substrate supply chain requests of reducing manufacturing cost, but usage is currently low due to application challenges for plating uniformity and limited packaging design adoption. Plating uniformity and specifically feature planarity, which measures how flat the tops of the traces, pillars, and vias are, represent important qualifying features of a copper plating process. A non-planar surface with fine traces could result in signal transmission loss, distortion of the connecting points, and possibly result in a device failure. In pillar plating and RDL applications, non-uniform surfaces require a planarization step after plating that adds additional processing steps and costs. Therefore, a copper plating solution providing uniform, planar profile without any special post treatment is highly desirable to fabricators. Due to the wide array of package designs being utilized today, which may include many kinds of features in advanced packaging, fabricators are interested in the ability to use one plating line to process multiple designs. In such a case, a single line / plating tool may be able to plate different features would be very useful.

With this specific additive package, we designed a system that can plate RDL features and pillars, at different conditions. In both applications, high resolution height uniformity between features is necessary. This commonality allows one additive system to successfully meet the requirements of both applications. The electrolyte successfully plates RDL fine lines and pillars with a uniformity and coplanarity that meets industry requirements, at panel level scale. Hence, the process is suitable for high production volume with vertical continuous platers.

The acid copper electrolyte presented here contains the common ingredients widely used in the industry: copper sulfate, sulfuric acid, chloride ions, and organic additives. These additives play a crucial role in controlling the deposit distribution as well as the physical properties of the copper deposit. The general organic additives are the wetter (or suppressor), leveler, and brightener. The wetter works in the presence of chloride ion to adsorb on to the cathode and increase the effective thickness of the diffusion layer. Therefore, the plating current increases and the deposit becomes more uniform, and a densely packed copper deposit can be obtained without burning. This modified diffusion layer improves the distribution of the deposit especially in fine line plating. The brightener is also called the anti-suppressor and as the name implies, it reduces the suppression. Most importantly it also acts as a grain refiner to deposit copper with a fine grain structure in a random orientation. Therefore, the brightener has significant influence on final structure and physical properties of the deposit, such as tensile strength and elongation. The leveler is a mild suppressor that adsorbs onto specific locations, such as corners and peaks of base materials. This allows more nuanced control of depositing copper in and around specific features.

In the presence of a micro profile, the diffusion layer tends to be thin at the peaks and thick at the valleys. In this case the micro profile will be exaggerated if it is plated without a leveler. If a leveler is present, the plating on the peaks will be suppressed and the micro profile will be diminished. Therefore, each additive plays a key role to obtain plating uniformity and adequate physical properties.

The uniformity targets for both applications are difficult to meet and require precise control of the bath. The additive and electrolyte concentrations are critical, as expected, but we also found that current density and temperature play key roles in the profiles of the plated features. Utilizing current density and temperature as factors, in conjunction with the additive levels, allows us to control the deposited copper more precisely and achieve more uniform surfaces.

RDL Fine Line Plating

Our test panels had 25 µm of patterned dry film on the surface, creating fine line features and pads. Each panel was cleaned prior to plating. Panels were plated in a vertical continuous plater (VCP) and each panel underwent a pre-clean cycle of 1 minute in acid cleaner, 1 minute in DI water rinse, 1 minute in 10% sulfuric acid prior to plating.

The inorganic and organic concentrations are shown in Table 1, as well as the ranges of current density (CD) and bath temperature. These concentrations and conditions were determined to be beneficial for RDL fine line plating through a series of experimentation.

Table 1: Inorganic and organic component concentrations of electroplating bath used for RDL panels

	Component	Addition level / range
VMS	$CuSO_4$	100 g/L
	H_2SO_4	200 g/L
	Cl^-	60 ppm
Organic additives	Wetter	5 mL/L
	Leveler	10 mL/L
	Brightener	2.5 mL/L
Plating Parameters	Current Density	1.0 – 7.0 ASD
	Temperature	20 – 27 °C

In addition to the selection and optimization of the additives, the type of anodes in the VCP made a significant difference in our experiments. When the VCP was operated using soluble anodes, the plated height variations between fine lines and pads averaged 1.4 µm for the unit with fine lines having 7 µm width/spacing, and 2.19 µm for the unit with fine lines having 5 µm width/spacing. Switching to insoluble anodes decreased the plated height variations between fine lines and pads in all cases. Average values were all below 1.0 µm for both units with the same 7 µm and 5 µm line spacing. These results are shown in Table 2. Insoluble anodes provide other benefits over soluble anodes, including easier maintenance and the ability to plate at higher current densities. The capability to plate at higher current densities is not critical for the RDL application, however, it is beneficial for the pillar plating application.

Table 2. Plated height variations between fine lines and pads on RDL panel

EP Soluble anode	Line thickness(µm)				Pad thickness (µm)				Thickness variation R (µm)
Line width/space (µm)	1	2	3	avg.	1	2	3	avg.	(pad - line)
7/7	17.82	18.03	17.73	17.86	19.45	19.16	19.16	19.26	1.40
5/5	17.14	17.86	17.37	17.46	20.14	19.55	19.26	19.65	2.19
EP Insoluble anode	Line thickness(µm)				Pad thickness (µm)				Thickness variation R (µm)
Line width/space (µm)	1	2	3	avg.	1	2	3	avg.	(pad - line)
7/7	19.02	18.5	19.02	18.85	19.53	19.53	19.53	19.53	0.68
5/5	17.99	19.02	17.99	18.33	19.02	19.02	19.53	19.19	0.86

Figure 1 shows cross sections of samples plated with the EP package at the optimized conditions for pattern plating. The plating current density was 1.5 ASD and the plating time was 60 minutes to obtain a copper thickness around 20 µm. The plated height variation between fine lines of 5 and 7 µm and the pads was minimal, and a planar surface was obtained.

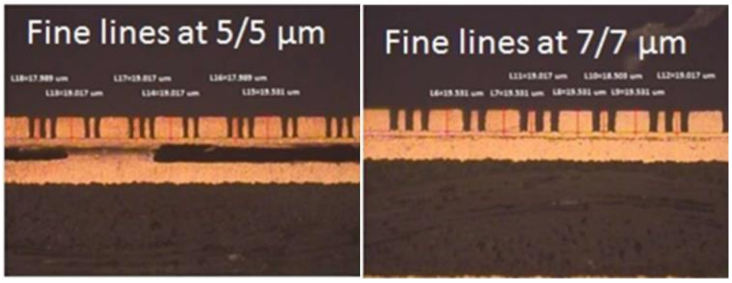


Figure 1: Cross sections of RDL panels plated with EP package.

The local height variation is very important to control, but the height variation across the panel must also be minimized. To quantify this, thickness variation was measured across the 410 mm x 510 mm panels at 3 points: top, middle to bottom, as shown in Table 3. For fine lines with width/spacing of 10 µm, the plated copper height variation was found to be below 0.5 µm, when plating under a current density of 1.5 ASD. When the current density was increased to 4 ASD, the thickness variation was approximately 1 µm. This was expected as it is commonly known that increasing the current density tends to increase plated height variation.

Table 3: Cu deposit thickness variation across panel.

	Pad height (µm)					Line height (µm)					R value (µm)
	1	2	3	4	M_n	1	2	3	4	M_n	$M_{n\ (pad)} - M_{n\ (line)}$
Top	19.43	19.54	19.49	19.43	19.47	18.76	18.98	19.15	19.32	19.05	0.42
Center	19.43	19.26	19.43	18.93	19.26	18.98	18.99	19.04	18.65	18.91	0.35
Bottom	19.82	20.10	19.77	19.88	19.89	19.71	19.60	19.71	19.48	19.63	0.26

Pillar Plating

The pillar plating application is inherently more difficult to achieve strict height uniformity with. The target surface copper is between 150 – 200 µm, whereas the RDL applications target around 15 – 20 µm. To achieve this high Cu thickness in a reasonable amount of time, the applied current density must be drastically higher. As stated earlier, higher current densities typically result in worse height uniformity within the features. The variation across the panel can also be very difficult to control at higher current densities, especially near the edges of the panel or when there are varying densities of features.

Each pillar is evaluated by measuring the difference in height of the pillar between the center and edge. The calculation is carried out using the equation in Figure 2. Various pillars are measured across the die and that variation is determined using the equation in Figure 3. The samples can be measured by encapsulating the sample in epoxy resin followed by cross sectioning, stripping of the dry film and then evaluating the Cu surface with SEM, or using a 3D profiler to analyze the surface topography with and without stripping the dry film. Through our evaluation, we used all the methods mentioned above and found that they were all in agreement.

$$Uniformity\ (WIF\%) = \left(\frac{Height\ \text{middle} - Height\ \text{edge}}{Height\ middle}\right) * 100$$

Figure 2: Equation for calculating profile of individual pillar (WIF%)

$$Uniformity\ (WID\%) = \left(\frac{Height\ \text{maximum} - Height\ \text{minimum}}{Height\ avg}\right) * 2$$

Figure 3: Equation for calculating uniformity (WID%) within the die

When the EP system was utilized to plate pillars, much higher current densities were applied. The target surface copper was significantly higher than in RDL applications, and so the plating durations were also increased. Fine tuning of brightener concentration, current density, and bath temperature allow control over the curvature of the tops of the pillars. Figure 4 shows three examples of how the curvature can be controlled. All three pillars are plated using EP system but controlling the plating parameters mentioned above allowed tuning of the curvature.

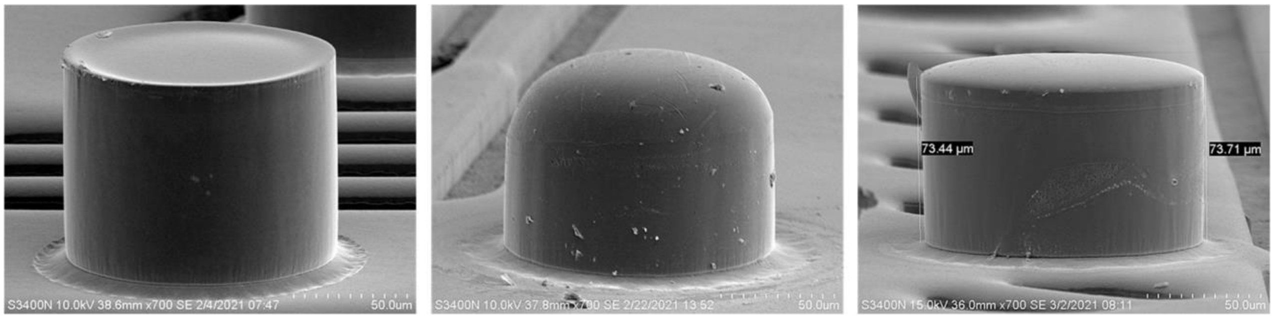


Figure 4: Examples from three experiments where the EP system produced dished, domed, and flat pillar tops.

An experiment was done to examine feature uniformity under current densities of 5 and 7 ASD, with plating times of 66 minutes and 44 minutes, respectively. A WYKO profiling instrument was used to measure the feature shape and plated uniformity within a die. The WIF uniformity was good, with all measurements below 3.5 µm under the process conditions. For the current density of 7 ASD, WIF% was below 4.7%, and it dropped further to below 2.0% when current density was reduced to 5 ASD. Table 4 and Table 5 contain the measurement data from both experiments.

Table 4: WYKO measurements of pillars plated at 5 ASD, for 66 minutes.

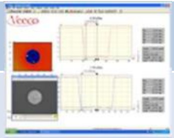
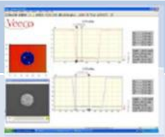
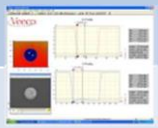
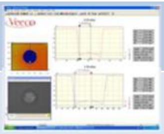
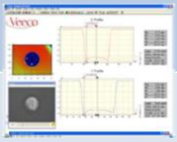
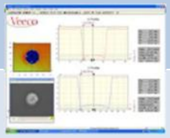
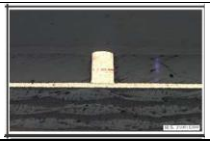
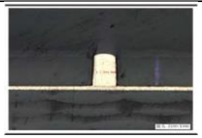
Location	Wyko measurement		WIF (µm)			Average (µm)
1	X axis		1.4	0.1	2	1.03
	Y axis		0.8	0.6	1.3	
2	X axis		1	2.17	2.66	1.46
	Y axis		0.19	1.69	1.1	
3	X axis		1.17	1.52	0.16	1.03
	Y axis		1.86	1.13	0.38	

Table 5: WYKO measurements of pillars plated at 7 ASD, for 44 minutes.

Location		Wyko measurement	WIF (µm)			Average (µm)
1	X axis		0.74	2.18	3.42	2.59
	Y axis		1.95	4.5	2.77	
2	X axis		4.41	3.6	2.37	3.5
	Y axis		5.03	2.7	3.35	
3	X axis		3.35	3.38	2.11	2.18
	Y axis		1.41	0.63	2.25	

To test the uniformity within a die, a panel with differing diameters of pillars and pads was used. This panel was plated at a current density of 7 ASD for 170 minutes to obtain a pillar height of 200 µm. The uniformity of pads and pillars was excellent, with a variation of only 1.3%. Table 6 shows a couple examples of specific pads and pillars, along with their measurements.

Table 6: Evaluating uniformity within a die.

Unit	1A	1B	Unit	1A (µm)	1B (µm)
Pillars, 150 µm diameter			Pillar	205.8	211.4
			Pad	210.7	208.6
Pad, 400 µm diameter			Average	208.3	210.0
			WIU	4.9	2.8
			Uniformity	1.3%	

To evaluate the larger scale uniformity, a 410 x 510 mm panel was sampled at seven locations. The locations of the samples are shown in Figure 5A, which also contains the average plated thicknesses at each point. Figure 5B contains the data from each location. The uniformity at each location was very good, with the maximum WIU% being 1.1%. The overall uniformity within this panel was about 7.1%.

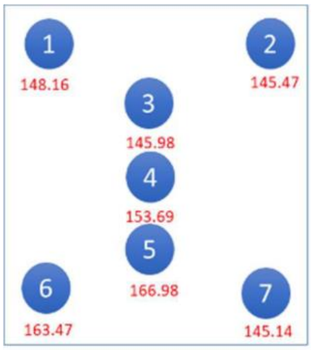
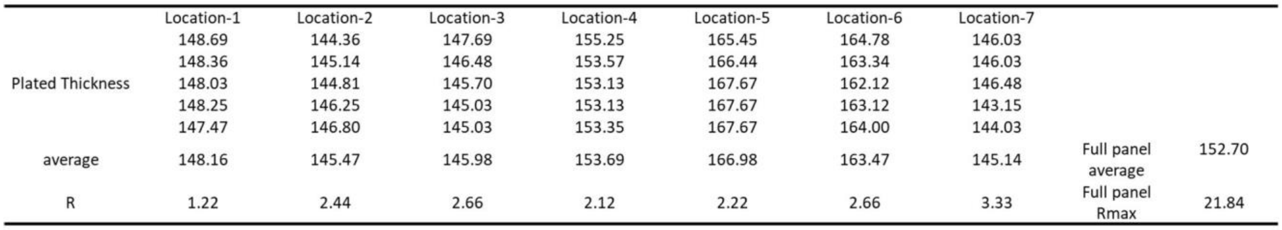


Figure 5A: Sample location on 410 x 510 mm panel



	Location-1	Location-2	Location-3	Location-4	Location-5	Location-6	Location-7		
Plated Thickness	148.69	144.36	147.69	155.25	165.45	164.78	146.03		
	148.36	145.14	146.48	153.57	166.44	163.34	146.03		
	148.03	144.81	145.70	153.13	167.67	162.12	146.48		
	148.25	146.25	145.03	153.13	167.67	163.12	143.15		
	147.47	146.80	145.03	153.35	167.67	164.00	144.03		
average	148.16	145.47	145.98	153.69	166.98	163.47	145.14	Full panel average	152.70
R	1.22	2.44	2.66	2.12	2.22	2.66	3.33	Full panel Rmax	21.84
%WIU	0.4%	0.8%	0.9%	0.7%	0.7%	0.8%	1.1%		

Figure 5B: Panel level uniformity data at each sample location

Copper Deposit Physical Properties

Physical properties of the plated copper deposit are essential for the reliability of the completed device. Tensile strength, elongation %, and internal stress are the key factors that we evaluate to predict the reliability of deposited Cu in fully fabricated devices. These properties are indicative of the Cu deposit's tolerance to thermal stress and warpage. The wetter, leveler, and brightener influence the physical properties of the deposit. Standard testing equipment was used to measure the tensile strength, elongation %, and internal stress. Tensile strength was above 40,000 psi and elongation% was above 18%. Internal stress is an important parameter when plating thin RDL. With high internal stress, the deposit may warp, and warpage may get worse with time or temperature. The internal stress of the plated deposits using system at current densities of 1, 4, 10 and 15 ASD was measured, and all exhibited low stress below 1.0 Kg/mm2 after annealing at 180 °C for one hour. The internal stress measurements are shown in Figure 7.

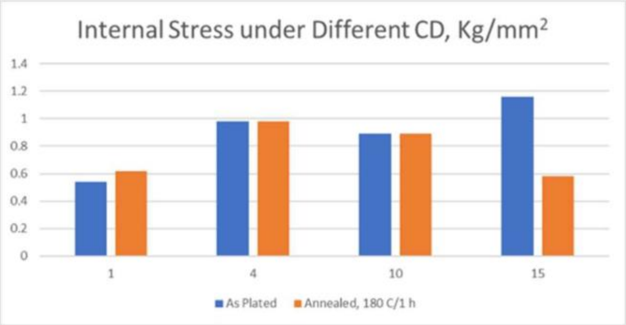


Figure 7: Internal stress measurements of EP deposits plated at 4 different current densities.

After the mold compound process, a thermal stress test was carried out. The sample was dipped in 288°C solder, 60 times. No separation was observed from scanning acoustic microscope (SAM) inspection as shown below in Figure 8.

Figure 8: Panels before solder dip (left), Panels after solder dip (right), inspected by SAM

Copper Deposit Grain Structure

An X-Ray Diffraction (XRD) study was performed on Cu deposits plated with the EP system at a current density of 1.5 ASD to identify the crystal phase and different planes. The diffraction pattern obtained was the same as the standard reported in the literature. The crystallographic densities and lattice constant were also in agreement with literature values. The data indicates that the deposits from the bath have preferred [111] planes as shown in the Table 7.

Table 7: XRD evaluation results of EP vs. Literature

Various data	Lit. Value Cu	EP
111	100	100
200	46	11.4
220	20	10.7
311	16	5.5
Lattice constant a [Å]	3.615	3.609
Density [g/cm^3]	8.92	8.98
Stress [MPa]	----	-6.7 ± 4.7

The FIB-SEM analysis was performed on samples that were deposited at 4 different current densities. All the images show equiaxial grain structure, regardless of the current density used to deposit the copper. The SEM images are shown in Figure 10 with their respective current densities.

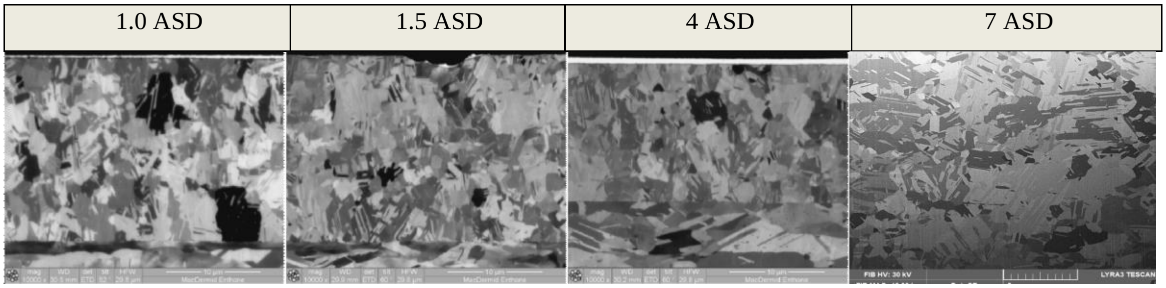

1.0 ASD
1.5 ASD
4 ASD
7 ASD

Figure 10: SEM images of Cu deposit from different current densities.

CONCLUSION

We presented copper plating processes for fine line plating and pillar plating for package substrates. The objective was to achieve coplanarity and uniformity within unit and within panel. The electrolyte utilized demonstrated the capability to plate fine lines with excellent coplanarity between the fine line feature height and pad feature height. The electrolyte also showed great uniformity on pillar plating when higher current density was employed. Through our experiments we found that with the same additive package, pillars could be produced with dished, flat, or domed surfaces. The physical properties, tensile strength, and elongation, meet IPC class III specifications. Low internal stress was shown for both applications as plated and after annealing. All the additive components were able to be analyzed with Cyclic Voltammetry Stripping (CVS) analysis.