

Double Side Sintered IGBT + FRD, 650V/ 200A, in a STO247 Package for High Performance Automotive Applications

Francois Le Henaff¹, Gustavo Greca¹, Paul Salerno¹, Jeffrey Durham¹, Monnir Boureghda¹, Anna Lifton¹, Jean Claude Harel², Satyavrat Laud², Weikun He³

¹Alpha Assembly Solutions, 109 Corporate Boulevard South Plainfield NJ 0890, USA

²Renesas Electronics America (REA), 2801 Scott Blvd, Santa Clara, CA 95050 USA

³Mentor Graphics 46871 Bayside Pkwy, Fremont, CA 94538 USA

Abstract

Double side sintered STO247 type packaged devices from Renesas Electronics America (REA) (tentative part number: *xJH6501DPz*, currently under development) are benchmarked against the leading device on the market used in high performance electric cars. The Renesas component utilize 650V, 200A rated IGBT die co-packaged with a similarly rated companion FRD die. Both components are interchangeable on the same board footprint, since the dimensions are approximately the same. Samples of both devices were tested at a delta T_j of 85°C and the *xJH6501DPz* proved to be at least 12 times more reliable than the leading device on the market (which failed at around 12k cycles and the Renesas parts are still electrically functioning and within target specification after 150k cycles). The fully sintered Renesas STO247 packaged samples were also subjected to a delta T_j of 110°C and demonstrated no signs of failure, even after 350k cycles.

Introduction

The reliability requirements for packaged single die IGBTs and IGBT die + Diode die in a single package are becoming more severe, particularly in demanding applications such as EV/HEV/PHEV inverters. Widely available and standard off-the-shelf TO247 and similar packaged devices are hard pressed to meet such requirements given the significantly higher power density levels in these applications that devices are subjected to over their operating life.

Several new device technologies are emerging in the market to address the performance and reliability requirements more effectively. Wide band gap material based devices are one such example, offering the promise of pushing the performance envelope set by silicon based

devices today. Silicon based IGBTs and FRDs are themselves being designed to enable further reduced losses, compared to what is achievable with state of the art technology today.

However, these technological advances will be limited if advances in attachment methods do not evolve as well. The commercialization of new packaging technology has proven to be a complex process. Silver sintering has attracted a lot of interest over the last decade and has shown the promise and ability to fulfill existing and in future more stringent reliability and manufacturability requirements. Argomax® silver sintering paste and film technologies are being developed by Alpha Assembly Solutions for die attachment purposes and allow a fast, low-pressure process for a wide range of applications including Power, RF, and high power LEDs.

The classic TO247 package structure using wire bonding and a copper tab has some major limitations when inductance and heat dissipation aspects are critical to the application. The use of silver sintering and a wire bondless structure has proven to permit a die temperature reduction of approximately 30%, which significantly increases the reliability of the component, enables better performance, and allows for a much higher power density of design. Such a new and radical design approach as implemented in the *xJH6501DPz* significantly improves ability for thermal management of the component since heat dissipation and extraction from the device is now possible from both sides of the die. In Figure 1 the differences on the internal structure of the components can be seen. Additionally, the epoxy mold compound was suitably redesigned to allow higher temperature operation (potentially up to 200°C; device currently targeted to operate up to 175°C, die temperature).

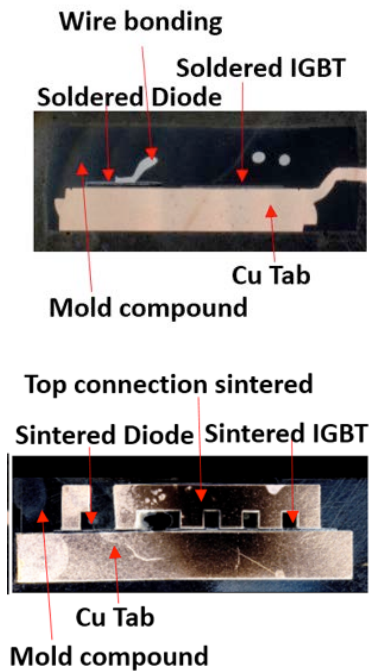


Fig.1: Top: Standard packaged component cross-section image. Bottom: New, Ag-Sintered packaged component, solder free and with Cu clip for the die top side connections.

Components and Test Methodology

The sintered packaged samples were subjected to thermal and power cycling stress profiles consisting of 200A current pulses, 15s ON/15s OFF, with a ΔT_j of $\sim 110^\circ\text{C}$, and ΔT_j of 85°C . For the standard packaged samples, the power cycling profile consisted of 130A current pulses, 15s ON/15s OFF, with ΔT_j of 85°C . The use of silver sintering and a wire bondless package design was proven to permit a die temperature reduction of approximately 30%; which enhances the reliability of the device and consequently of the inverter of which it is an integral part. Further, the reduced parasitic inductances enables potential for significantly improved electrical performance, and lower operating losses, thus allowing a much more compact inverter design.

The REA designed packaged components utilize an 8.8 mm x 8.8 mm, 650V/200A rated IGBT die, and an 8.8 mm x 5.1 mm, 650V/200A rated FRD die, both from Renesas Electronics Corporation (REA). The dies were sintered (90s, 250°C , 10MPa) on a custom designed Cu tab and lead frame using Alpha's Argomax® 8030/35 wafer level film technology, where the sinter material can be adhered to the back of the semiconductor wafer prior to dicing. Copper clips

were sintered (90s, 250°C , 10MPa) to the die top using Argomax® film technology as well. The power cycles tests and thermal impedance measurements were performed using the Mentor Graphics MicReD 1500A tester.

A cross section of a sample at t_0 cycles shows the clip and die attach interfaces after sintering. (Figure 2). Density in the top and bottom layers is approximately 90%.

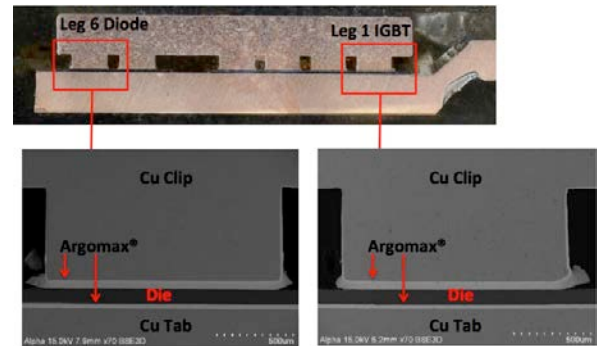


Fig.2: New, Ag-Sintered packaged component after assembly; note the highly uniform sintering layers, with no visible die tilting or cracking issues.

The MicReD Industrial 1500A Power Tester from Mentor Graphics runs a calibration of the VCE (collector to emitter voltage) to understand if the variations on the measurements during the power cycling test are indicating a failure on the die attach or on the top electrical connection (wire bonding on the standard component and clip on the new one).

The sample DUTs are mounted in custom tooling for test with thermal grease (G751 from ShinEtsu Group) filled with silver particles to improve the thermal path. A torque wrench and consistent application of thermal grease was used to ensure uniform and consistent pressure was applied to all devices on the cooler sink.

The cooling liquid was kept at 60°C at all-times throughout the tests and 3 components are arranged in series through the same cooling circuit, as showed in figure 3.

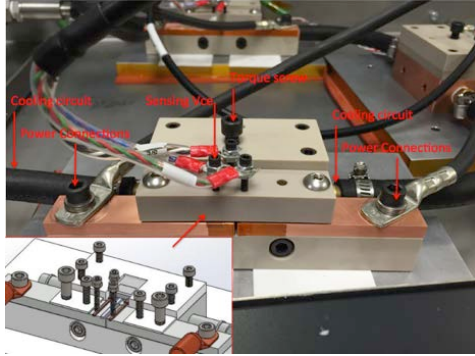


Fig. 3: Test setup for Rth measurement and power cycling test. All the DUT are mounted on the fixture using the same TIM (Thermal Interface Material) thickness, same pressure is applied in each component by the torque screw.

The thermal resistance of both sets of sample components was performed initially, separating out the values of each layer of the internal structure to clearly understand the advantages of using the silver sintering and wire bondless approach. This measurement was repeated at each 10k cycles to be ensure detection of the beginning of a failure and drive metallographic investigation afterwards (Fig. 3). Each drop of the T_{jmax} during the test as seen in the data is due to the Rth measurement being performed at that time. During the test the VCE (collector to emitter voltage) is also continuously measured.

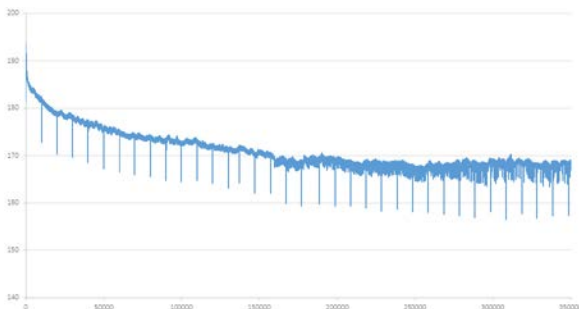


Fig.3: T_{jmax} measurements of the sintered DUT for a Delta T of 110°C. Each drop of T_{jmax} correspond to the Rth measurement every 10k cycles.

Once Rth measurement is finalized, the DUT are subjected to a fixed current in order to reach consistent Delta T_j .

The standard TO247 packaged components were subjected to 130A to reach 85°C delta T_j , during 15s and then to a 15s relaxation period. The double side sintered STO247 packaged components were subjected to 200A during 15s and then to a 15s relaxation period in order to

achieve same 85°C delta T_j . Both components were driven by a gate voltage of +20V to ensure minimum possible saturation voltage across the IGBTs. To evaluate a higher delta T_j , the sintered package components were also subjected to a +15V gate voltage to dissipate more power and achieve a delta T_j of ~ 110°C. When subjected to 200A pulses, these components reached a peak temperature between 142°C to 145°C. It can be noted that the standard packaged components reached the same peak temperature when subjected to 130A current pulses. When the double sided sintering components were subjected to +15V gate voltage the peak die temperature increased to ~ 170 °C. Nine sample components of each type were tested until failure.

Test Results and Discussion

Thermal measurements for the two sets of sample components showed a significant improvement on the junction-to-case thermal resistance for the new sintered wire bondless component. These results indicate a 42% reduction in this parameter compared to the standard component. Through the use of Alpha's Argomax® sintering technology, it is possible to reduce the die attach layer to 25µm instead of 75/80 µm found in the standard solder attached product. The thermal conductivity for the Argomax® sintered product was measured 5.2X higher at 260W/m.K, than that for typical solder. On the 85°C delta T_j , 100% of the solder attached components failed in less than 12k cycles, with current pulses being 130A. The typical failure mode was bond wire lift-off that became evident from a severe variation on the Vce and delta T_j during the power cycling test (Fig. 4 and 5). 27 components were subjected to power cycling as described in Table 1.

Components	Test conditions	Delta T°C	Quantity
Std TO247	20V Vg; 130A 15s on/15s off	85	9
New TO247	20V Vg; 200A 15s on/15s off	85	9
New TO247	15V Vg; 200A 15s on/15s off	100	9

Table 1: Components tested in active power cycling.

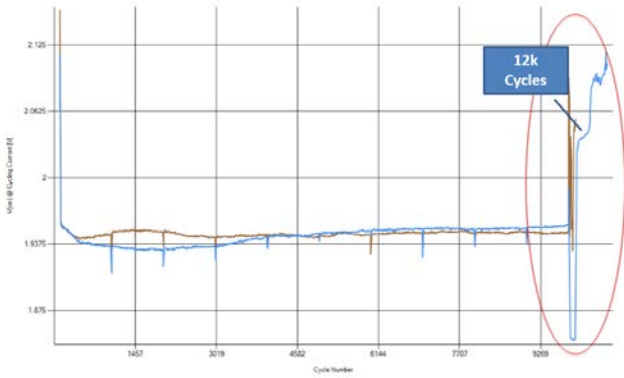


Fig.4: Vce continuous measurement during active power cycling test for soldered components, 2 best cases presented. Failure by 12k cycles, demonstrated by a spike on the Vce value, typical signature of bond wire related failure.

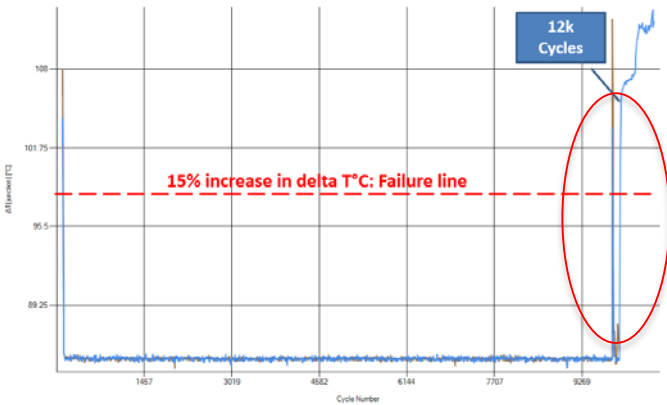


Fig.5: Delta Tj results after active power cycling test for soldered components, 2 best cases presented. Failure by 12k cycles, demonstrated by a spike on the Delta Tj.

On the Argomax® sintered component, 100% of the parts survived for 150k cycles for the 85°C delta Tj class and 350k cycles for the 110°C delta Tj class. Both tests were stopped, without any observed failures in these devices.

Further analysis on sample devices after 150k cycles (85°C delta Tj) and 350k cycles (110°C delta Tj) showed no degradation of the sintered layers (Fig. 6).

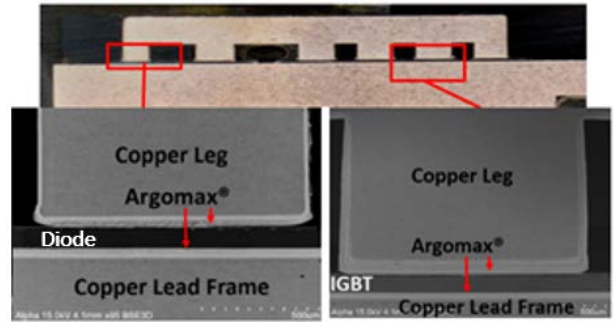


Fig.6: Cross section done in a part after 150k Cycles (85°C delta Tj), no degradation on the clip and die attachments were observed.

There was a minor density increase observed on the silver sinter interfaces from t_0 cycle to $t=350k$ cycles. The average measured (5 parts, 10 connections) density in the interfaces increased from 87% to 93% after 150k cycles (Figure 7) and from 87% to 94.2% after 350k cycles which explain the slight decrease of Delta Tj during the test because the density increased and the thermal path resistance decreased along the test period (Fig. 8).

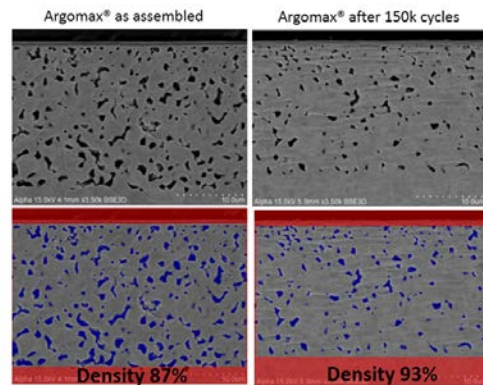


Fig.7: Density measurement on a part at t_0 cycle and after 150k Cycles (85°C delta Tj).

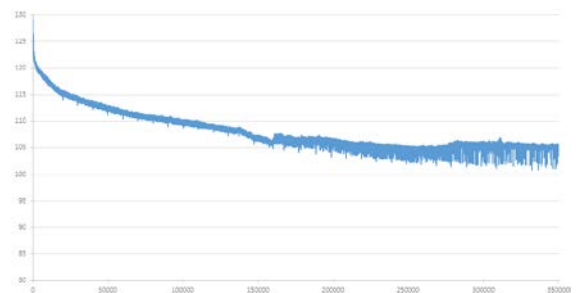


Fig.8: Delta Tj variation during test for 110°C Delta Tj devices, Rth measurements also presented each 10k cycles.

The cumulative structure function measured at every 10k cycles (Fig. 9) helps understand the benefit of using silver sintering technology as an assembly process. The structure function here presented (thermal capacitance vs. thermal resistance for the path going from the junction to tab of the component) shows relatively stable values for thermal capacitance along with a decrease in thermal resistance (0.0220 °C/W at t0 cycle and a 0.0175 °C/W at 350k cycles). The drop of almost 20% in thermal resistance is explained by the increase of density in the sintered layers during cycling. The tests conducted on the sintered devices for 85°C and 110°C delta T_j clearly demonstrate significant improvement in thermal performance and consequent lifetime improvement compared to standard solder attached and wire bonded TO247 packaged components.

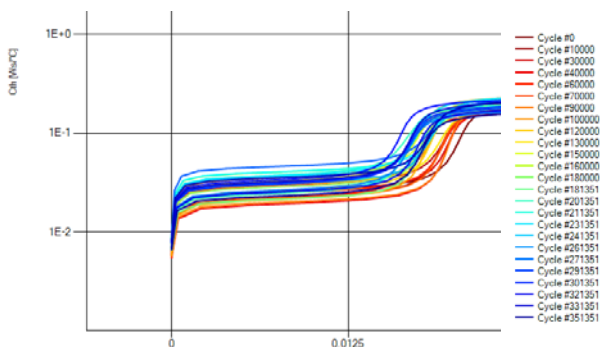


Fig.9: Cumulative structure function of the device throughout the 350k cycles for 110°C Delta T

Conclusions

The reliability of the Argomax® sintered component is shown to be at least 15X higher than that for the standard packaged components tested using 85°C delta T_j gradient. Additionally, Argomax® sintered components can carry 53% more current and still achieve same maximum junction Temperature (145°C). The new sintered die components continue to be functional, even after 150k cycles.

The tests conducted at 110°C delta T_j gradient on the sintered die components showed no failure despite being subjected to 350k power cycles. Peak junction temperature was measured at ~ 170°C throughout the test, which means Si devices can be pushed to a higher operating temperature levels (close to rated maximum of 175C) without any adverse impact to key electrical parameters

and performance and enable a further significant extension of the performance envelop of current and future generation of Si and wide band gap technology devices.

When combined with a high performance die, The use of Argomax® 8030/35 wafer level lamination for die attach combined with laminated Argomax® 8020 sinter film to the clip attach can enable a lower peak junction temperature, higher reliability, compact design and a more cost effective cooling system.

References

- [1] U. Scheuermann et al. "The road to the next generation power module: a 110% solder free design", CIPS'2008.
- [2] F. Le Henaff et al. "Reliability of Double Side Silver Sintered Devices with various Substrate Metallization" PCIM 2016.
- [3] Ikeda, Y. et al. "Investigation on Wire-bondless Power Module Structure with High-Density Packaging and High Reliability, International Symposium on Power Semiconductor Devices and IC's." 2011, Proceeding CD, p.272-275.
- [4] Horio, M. et al. "New Power Module Structure with Low Thermal Resistance and High Reliability for SiC Devices." PCIM Europe. 2011, Proceeding CD, p.229- 234
- [5] Horio, M. et al. "Ultra Compact high reliability SiC MOSFETs Power Module with 200C Operating Capability, ISPS, Bruges 2012.