Microvia Reliability
Key Issues and Preferred Processes

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INTRODUCTION
The microvia structure has enabled circuit miniaturization for decades and continues to be the single most important interface in the electronic design. As reliability becomes increasingly important, the ability of these structures to hold up during the stresses of assembly and during end use is under extreme scrutiny. MacDermid Alpha Electronics Solutions has been the partner to the industry for years and has developed electronics manufacturing processes that can produce consistent electrical structures. We have been working to understand the microvia structure and all of its interfaces, failure modes, and ways to improve. Presented here are the key issues and our preferred process selection for the microvia reliability solution.

DIRECT PLATING PROCESSES: BLACKHOLE, ECLIPSE, SHADOW, AND ENVISION
Reduce Copper Interfaces, Improve Yields, and Enable Higher Quality

Direct plating technologies are used widely in electronics manufacturing as an alternative to electroless copper for activating drilled through holes and vias for electroplating. These processes are environmentally friendly and allow a range of benefits compared to electroless copper in terms of cost and quality enhancements to the board design. Blackhole, Eclipse, and Shadow are industry leading processes that coat the surface of the microvia wall with conductive carbon, while ENVISION HDI uses a conductive polymer.

Direct plating allows for a single interface of electrolytic copper to the microvia target pad, eliminating the need for flash plate and electroless copper and reducing the number of potential separation points. The low-etch direct metallization processes Blackhole LE and Eclipse LE are especially well suited to the challenges of mSAP for SL-PCB and IC substrate designs.

<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th>Low Build &amp; Flash</th>
<th>High Build Cu</th>
<th>Blackhole LE / Eclipse LE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Laminate Prepreg &amp; Cu Foil</td>
<td></td>
<td>3 µm</td>
<td>3 µm</td>
<td>3µm</td>
</tr>
<tr>
<td>LDD Oxide Laser Drill De-Oxide</td>
<td></td>
<td>3 µm -0.5 -0.5 = 2 µm</td>
<td>3 µm -0.5 -0.5 = 2 µm</td>
<td>3 µm</td>
</tr>
<tr>
<td>Desmear Metallization</td>
<td></td>
<td>2 µm - 0.5 + 0.5 + 3 = 5 µm</td>
<td>2 µm - 0.5 + 1.0 = 2.5 µm</td>
<td>3.0µm - 1.0 = 2.0 µm</td>
</tr>
<tr>
<td>Pattern Image Develop</td>
<td></td>
<td>5 µm</td>
<td>2.5 µm</td>
<td>2.0 µm</td>
</tr>
<tr>
<td>Pre-Clean Cu Via Fill</td>
<td></td>
<td>5 µm / +20 = 25 µm</td>
<td>2.5 µm / +19.5 = 22 µm</td>
<td>2.0 µm / +19 = 21 µm</td>
</tr>
<tr>
<td>Strip Resist Flash Etch</td>
<td></td>
<td>0 µm / -7 = 18 µm</td>
<td>0 µm / -4 = 23 µm</td>
<td>0 µm / -3 = 18 µm</td>
</tr>
<tr>
<td>Layers of Cu to Flash Etch</td>
<td></td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

Carbon and graphite technology have co-evolved with HDI to solve manufacturing challenges like mSAP copper etch budget allowing for a reduced copper thickness at the final flash etching step.
ELECTROLESS COPPER TECHNOLOGIES: M-COPPER OMEGA, VIA DEP 4550, SYSTEK SAP

Horizontal and Vertical Processes, Multiple Palladium Activator Technologies, and Low Deposit Stress

Electroless copper has been the primary metallization of choice for making through holes and vias conductive for decades. Our extensive suite of chemistries includes the low-stress horizontal or vertical Via Dep 4550, and premium M-Copper Omega processes for HDI manufacturing. The Systek SAP is a high-performance primary metallization process for IC substrate scale designs.

![M-Copper Omega Backlight](image)

We offer a choice of ionic or colloidal palladium activators both with exceptional activation as measured with backlight coverage.

![Via Dep 4550](image)

Via Dep 4550 provides the optimal grain structure at the target pad interface for reliable microvias.

ELECTROLYTIC COPPER PLATING SOLUTIONS: VF, AVF, VF-TH, UVF SERIES

Copper Microvia Filling Technology Tailor Matched for Preferred Grain Structure Across Interfaces

Through our extensive experience in the via filling technologies arena, we have developed highly reliable copper microvia filling processes that pair specifically with our electroless and direct plating primary metallization processes. When combined in unison, an exceptional grain boundary can form through self-annealing, resulting in lasting microvia structures that hold up to extensive cycling and end use stressors. For standard PCB and HDI, the MacuSpec VF and AVF Series are industry leading processes for copper microvia filling. For advanced HDI, and Substrate-Like PCB, the MacuSpec VF-TH Series baths can simultaneously plate through holes and fill copper microvias. For IC Substrate manufacturing, the Systek UVF Series can plate 2 in 1 RDL layers with exceptional co-planarity.

![VF + MacuSpec VF-TH 200 Via Fill](image)

Via Dep 4550 Electroless Copper + MacuSpec VF-TH 200 Via Fill

The low-stress Via Dep 4550 enables thermomechanical benefits compared to regular electroless copper processes and can provide optimal grain structure at the via interface.

![Blackhole + MacuSpec VF-TH 200 Via Fill](image)

Blackhole Direct Metallization + MacuSpec VF-TH 200 Via Fill

Compared to standard electroless copper plating, the via interface with Blackhole direct metallization is simpler and has fewer areas for reliability concern, while also allowing for environmental benefits.
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A PORTFOLIO OF ROBUST PROCESSES FOR IMPROVED VIA INTERFACES

<table>
<thead>
<tr>
<th>PROCESS SEGMENT</th>
<th>BOARD TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Main Category</strong></td>
<td><strong>Subcategory</strong></td>
</tr>
<tr>
<td>Primary Metallization</td>
<td>Direct Metallization</td>
</tr>
<tr>
<td>Electroless Copper</td>
<td>M-Copper Omega, Via Dep 4550</td>
</tr>
<tr>
<td>Electrolytic Metallization</td>
<td>Via Filling Copper</td>
</tr>
</tbody>
</table>

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