MSL-1 reliability performance in QFN packages using no-bleed die attach

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With the advent of autonomous technologies, the semiconductor industry requires a new paradigm of reliability. Certainly, the biggest driver is the goal of autonomous driving, where reliability cannot be sacrificed. To this end, many suppliers are combining businesses to synergize novel approaches to deliver the highest reliability.

Perhaps the principal failure mechanism in chip packages is delamination. The primary causes for delamination arise from issues with thermal expansion and moisture intrusion. Initially, it was believed that controlling thermal expansion coefficients of packaging components was all that was needed. Indeed, for small packages this appears to be true, but as packages become larger and more complicated, it becomes very difficult to control the coefficient of thermal expansion (CTE) of every component.

Attempts to improve reliability by increasing mold compound adhesion have led to maximizing the surface area of the interface between the mold compound and the lead frame. Unfortunately, this led to the unintended consequence of increased resin bleed from die-attach adhesives, which in turn led to failure of the adhesives and delamination under the die. With a plethora of adhesives from multiple suppliers, it becomes difficult to find a "one size fits all" correction for the resin bleed.

By successfully implementing conductive film type die attach, the resin bleed out (RBO) issue becomes nonexistent, eliminating the need for a lead frame surface treatment that can eliminate RBO from all adhesives. More complex packages with multiple dies and high I/O counts are becoming commonplace. Many of these systems in a package (SiP) utilize hybrids of solder die attach and traditional die attach or multiple curing cycles to stack dies. This article reviews some of the critical factors that lead to delamination within a chip-scale package, and methods that alleviate these causes.

Package reliability requirements

As the complexity of various technologies advance, semiconductor package reliability requirements are continually increasing. What once required three or more chip packages, now must be achieved by one so as to pack more I/Os into smaller and smaller volumes. The capabilities of a desktop computer from the 20th century are now housed in a mobile phone that can fit in your pocket. This was made possible by producing chip packages that contain multiple chips, thereby generating more functionality in a single component – a system in a package (SiP). These SiP packages come in a variety of designs: stacked die, side-by-side, or multi-chip fan out, with variations of the same. Each of these designs exhibits its own set of manufacturing issues that can impact reliability. While organizations such as JEDEC, IPC, and AEC define classifications and tests that these parts must pass to qualify for their acceptance, many manufacturers test at even more stringent conditions to ensure the dependability of their production.

In addition to the above consideration, more complex wafers are designed with increased capabilities that require higher lead counts with tighter spacing. In these cases, the chip to die-attach pad area ratio becomes critical. As the area ratio decreases, the chance for delamination at the lead frame-mold compound interface increases. Delamination tests and electrical testing are critical measures of reliability. To achieve higher reliability levels, units are stressed in higher temperature, higher humidity, or extreme thermal cycling tests to verify that production meets pre-determined standards. This article will discuss some of the important issues impacting reliability and solutions that have been developed to overcome them.

Adhesion/delamination

One of the most common problems faced by packaging houses is delamination. Delamination can occur between epoxy mold compound and the lead frame, between the die and lead frame, or between the die and mold compound. To enhance adhesion at the lead frame interface, various roughening techniques have been employed. The two most popular are quite different. One is a subtractive process – etching, and the other is an additive process – electroplating.

The additive process typically uses controlled electroplating conditions to generate a roughened deposit of copper. Because it has been reported that copper and copper oxides can cause decomposition of epoxy resins at elevated temperatures, the reliability of this surface has been questioned unless coated with another material to reduce the impact of copper on the mold compound.

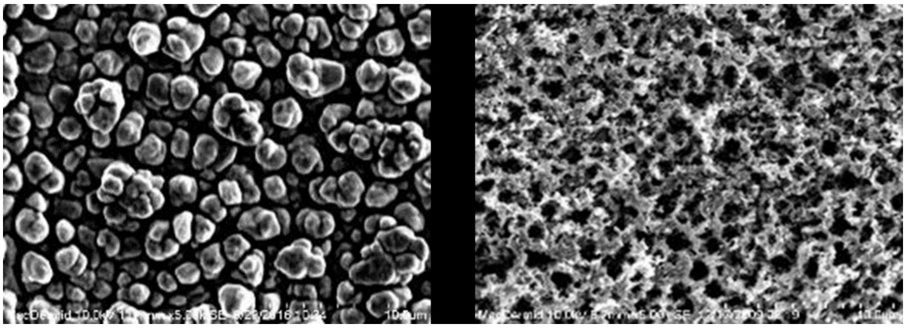

Figure 1: SEM photo of an additive process (left) and a subtractive process (right).

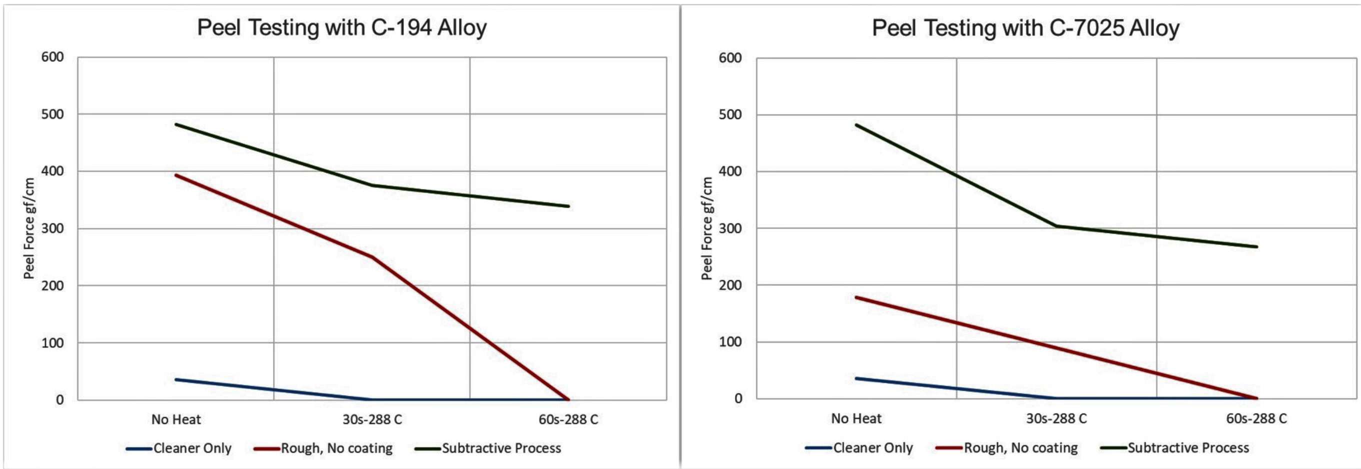

Figure 2: Graphs showing the peel strength of treated and untreated alloy surfaces.

Figure 3: Alloy surface after MSL-1, reflow, and button shear—untreated on the left, treated on the right.

The subtractive process utilizes a special micro-etching composition that concurrently etches a rough morphology and deposits an adhesion-promoting coating. The advantage of this process is that it can be run in the packaging house after die attach. For some SiP configurations, this can be beneficial, whereas plating a conductive copper coating over the entire area will, after die attach, lead to shorts within the package. The subtractive process will not catalyze epoxy decomposition at higher temperatures because the coating that is deposited isolates the copper surface from the molding compound. The differing morphologies of these two processes are shown in Figure 1.

Adhesion tests on roughened surfaces with and without the adhesion-promoting coating, compared to no treatment at all, demonstrated the utility of the coating with respect to adhesion after high-temperature treatment. The peeling force to remove a one-centimeter wide strip of lead frame alloy from a cured epoxy surface is illustrated in Figure 2. The results demonstrate that the coating is critical for maintaining adhesion at the extreme temperatures tested. No treatment provides very little adhesion improvement compared to the roughened surfaces, but adhesion falls away quickly with temperature exposure unless the adhesion-promoting coating is included.

Button shear testing with epoxy mold compounds (G-600 and G-770 from Sumitomo-Bakelite) after moisture sensitivity level 1 (MSL-1) preconditioning followed by triple reflow at lead-free reflow temperatures demonstrated a similar improvement in adhesion, but also provided some evidence of the mechanism that generates improved resistance to moisture sensitivity. Observation of the alloy surface after the button has been removed (see Figure 3) shows a vivid difference. While the untreated surface shows an oxidized appearance, presumably from moisture ingress at the mold compound-lead frame interface, the treated surface remains clean and unchanged. This indicates that the process prevents moisture ingress, which would have led to delamination (popcorning) during reflow.

As discussed in [1,2], a rough surface leads to increased RBO. The most common solution for RBO coats the treated lead frame with a surface modifier to reduce surface energy, thereby inhibiting the flow of the resin. Because not all die-attach adhesives are the same, especially regarding surface wetting, anti-RBO processes must be carefully controlled for each adhesive used. The development of conductive-film die-attach materials that are applied to the wafer, and transfer with the chip to the lead frame, provides a more attractive approach to avoiding RBO.

Conductive film die attach

A conductive film die-attach process starts with the wafer lamination followed by dicing and die bonding. The die bonding is carried out on similar equipment as a standard epoxy die-attach process with slightly different settings to enable the wetting of the film to the roughened surface of

Figure 4: Process flow for conductive film die attach.

the lead frame. The schematic process flow is described in **Figure 4**.

ATROX® CF200-1D film is evaluated on roughened copper lead frames to determine the delamination resistance of the conductive film die attach after preconditioning. The assembled unit shows minimal to no fillet after bonding, which indicates no resin bleed out and a high rate of adhesion on the lead frame surface. To the contrary, the paste shows RBO on the lead frame surface. **Figure 5** illustrates the difference between RBO with liquid die attach compared to the "no-bleed" conductive film die attach.

Figure 6 shows a cross section image of the film after die bonding and encapsulation. The assembly settings used for the conductive die attach film process are tabulated in **Table 1**. The conductive film attach parts show very high adhesion results with superior delamination resistance after preconditioning. **Figure 7** shows THRU-Scan™ images of a quad flat no-leads (QFN) 5x5 device before and after being subjected to MSL-1 preconditioning followed by 3x reflows at a 260°C peak temperature. In comparison, **Figure 8** shows the THRU-Scan™ images of the same parts assembled using a standard paste with RBO; the images show delaminations after MSL-1 indicating that the root cause of failures is attributed to the paste's poor delamination resistance caused by RBO.

For conductive adhesives, the ratio of conductive filler to resin material is critical for maintaining physical properties. The RBO can weaken the composition of the adhesive under the die when the loss of resin increases the filler to resin ratio beyond its optimum range. This can lead to weakening of the adhesive under the die, and ultimately, delamination. Micro-sections of the die attach show that the conductive film has flowed into the roughened surface of the lead frame during the curing process (**Figure 9**). The ability for both the die attach adhesive and the epoxy mold compound to flow into the surface topography is a critical contributor to delamination improvement.

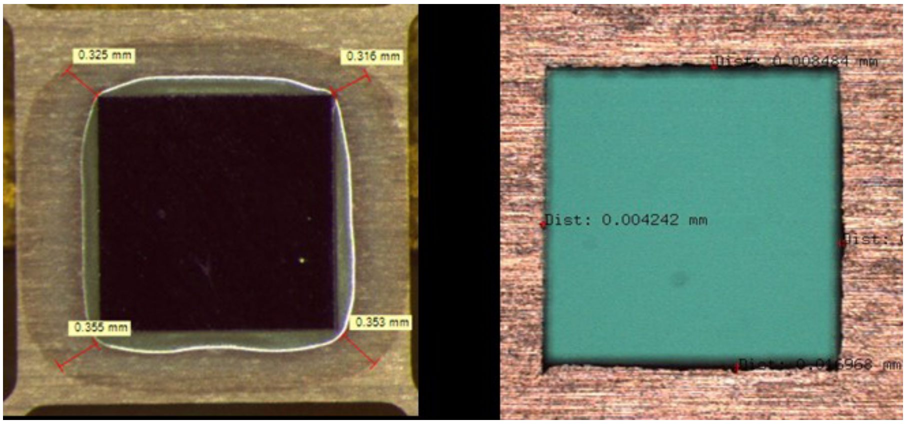

Figure 5: Conductive die attach paste showing RBO vs. conductive film die attach with no resin bleed.

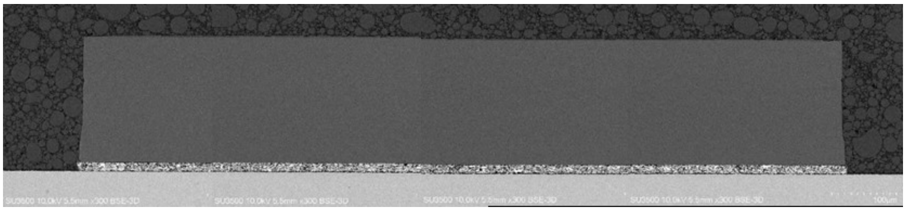

Figure 6: Assembled die on the lead frame using conductive film.

Process/Conditions	Lamination	Dicing	Bonding	Curing
Temp (°C)	75C-85C	<50C	90C-120C	>=175C
Pressure (N/mm2)	>0.3 N/mm2	None	>=1N/mm2	None
Time (min)	< 1 min	Die Size dependent	1 sec Max	120min

Table 1: Assembly settings for conductive film.

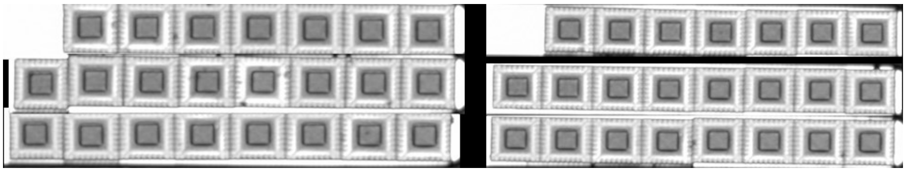

Figure 7: THRU-Scan™ images of conductive die attach film before MSL-1 (left) and after MSL-1 (right).

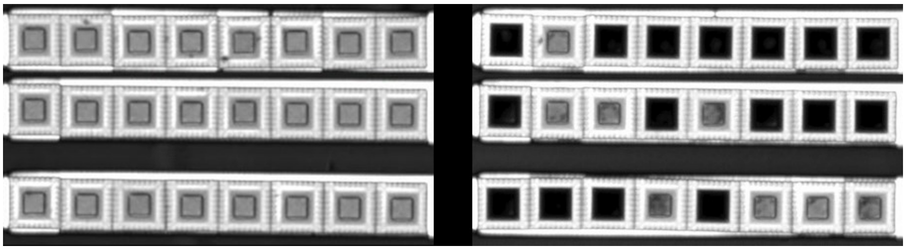

Figure 8: THRU-Scan™ images of die attach paste before MSL-1 (left) and after MSL-1 (right).

a)

b)

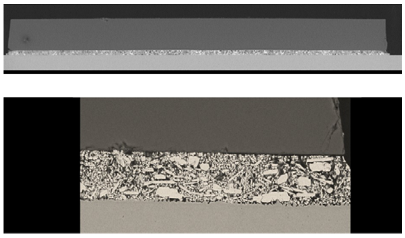

Figure 9: SEM photos of a micro-section of a conductive die attach film after MSL-1 showing: a) (top) a low magnification overview; and b) (bottom) higher magnification detail.

Summary

For many advanced microelectronics devices being used now or in the near future, failure can be catastrophic. Medical devices are now used to measure or control critical bodily functions. Automobiles equipped with autonomous driving capabilities are now asked to react to emergency situations, such as an impending collision. The assembly methods to produce the high reliability required need to be implemented now.

RBO is a constant concern but is extremely difficult to control because of the numerous die-attach adhesives that are commercially available from multiple sources. The resins used in these adhesives arise from various organic compounds. Additives are used to improve adhesion, wettability, filler stability, and RBO. The difficulty with controlling RBO with surface energy modifiers arises from the variety of resin chemistries.

The THRU-Scan™ images illustrate the weakness of poorly controlled RBO. Conductive film die attach is an elegant solution to the issue because it is applied as a solid that creates no RBO but flows into the morphology of the roughened surfaces during cure. The enhanced moisture resistance produced by the roughening mechanism delivers higher MSL reliability without the associated problem of resin bleed.

References

1. S. Kanagavel, D. Hart, "Optimization of die attach to surface-enhanced lead frames for MLS-1 performance of QFN packages (part 1)," *Chip Scale Review*, Mar/Apr 2017.
2. D. Hart, S. Kanagavel, "Optimization of die attach to surface-enhanced lead frames for MLS-1 performance of QFN packages (part 2)," *Chip Scale Review*, Jul/Aug 2017.

Biographies

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