

The Effects of Board Design on Electroplated Copper Filled Thermal Vias for Heat Management

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ABSTRACT

This paper discusses a through hole copper filling process for application in high density interconnect constructions on thin IC and LED substrates where high reliability and thermal management are essential. The process consists of a two step acid copper plating cycle. The first step utilizes periodic pulse reverse electroplating to form a conductive copper bridge across the middle of a through hole followed by direct current electroplating to fill the resultant vias formed in the bridge cycle.

The ability of the process to fill a variety of through hole sizes on substrates of varying thickness while minimizing the overall surface copper build up are critical in applications requiring efficient thermal management as circuit miniaturization continues.

The through hole fill technology and the results of a recent design of experiments investigating the effects of a variety of factors such as substrate thickness, through hole diameter, plating cycle, current density, and plating time will be presented in this paper.

Key words: PPR electroplating, via fill, thermal management, through hole fill

INTRODUCTION

Technological advances in electronics fabrication continue to push the boundaries to increase circuit density utilizing smaller and smaller interconnect structures such as stacked vias, buried vias, and via in pad (See Figure 1). Coupled with the use of higher power density devices on smaller and smaller board real estate, an extra dimension of thermal management arises requiring efficient methods of heat dissipation to ensure product performance and life.

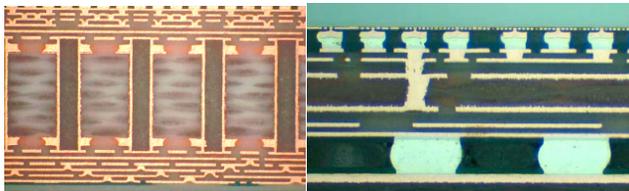


Figure 1. Paste Plugged Vias and Copper Filled Vias

The importance of heat dissipation is well known in the LED industry where a high operating junction temperature is

detrimental to product performance. At high operating temperatures, an LED's light intensity and color can be greatly affected and its expected life dramatically shortened (See Figure 2).

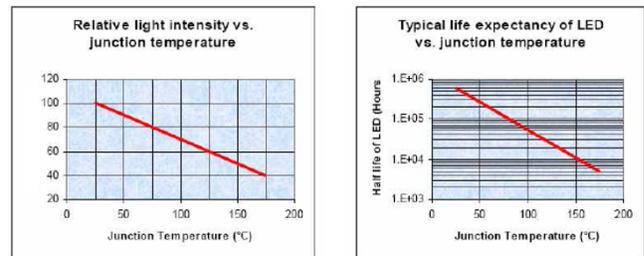


Figure 2. Effect of LED Junction Temperature on Intensity and Life

Several methods of heat dissipation have been successfully used to draw generated heat away from a component. These include the use of metal core printed circuit boards, plugged thermal vias, and copper filled thermal vias.

In the use of MCPCB's, the heat generating components are mounted onto a panel containing a core of copper, aluminum, or iron that effectively draws heat from the device and dissipates it into the surrounding environment. This is generally the most efficient method of heat removal and offers an additional benefit of RF shielding if the application requires. The cost of this method can be prohibitive for the application (See Figure 3).

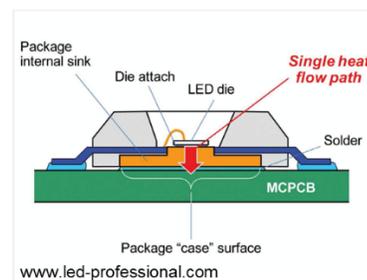


Figure 3. Example of Metal Core Printed Circuit Board

Plugged thermal vias utilize a metal-filled epoxy-based paste to increase the thermal conductivity of the through hole allowing heat transfer from the operating device to an underlying heat dissipation layer (See Figure 4). Though effective in certain applications, the use of this method is

limited due to the relatively low thermal conductivity of the metal-filled epoxy paste as compared to the pure metals (See Figure 5).

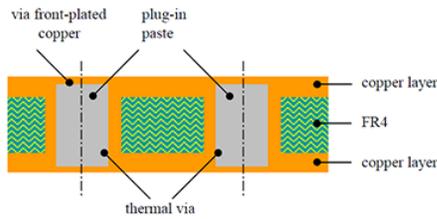


Figure 4. Plugged Thermal Vias

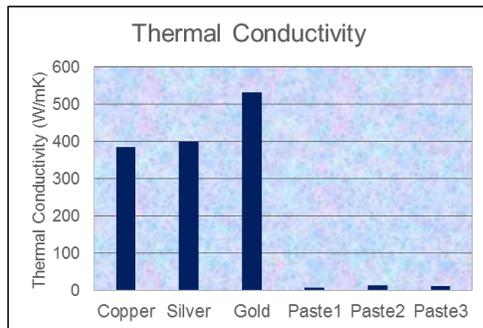


Figure 5. Relative Thermal Conductivities of Pastes versus Pure Metals

Copper filled vias utilize unique plating techniques to fully fill thermal vias with plated copper forming a solid copper plug. Advantages of copper filled vias include :

- Reduction in CTE mismatch of resin/paste plug
- Stable platform for stacking microvias
- Solid pillar structure within the through hole
- Lower likelihood of adhesion failure on the plated-over filled via
- High thermal conductivity of copper

New plating technologies were developed to completely fill through holes and vias in build-up core layers in HDI and IC substrates with solid copper. Among the approaches for filling through holes in a thin core board with copper was DC plating.

In this “two stage” technique, one begins with an X-shaped through hole. In the initial stage of plating, copper is preferentially deposited in the middle of the through holes until the growing copper deposits meet to form a bridge. The resulting double blind vias then fill to complete the copper filled through hole. Terms to describe this process are bridge and fill (See Figure 6).

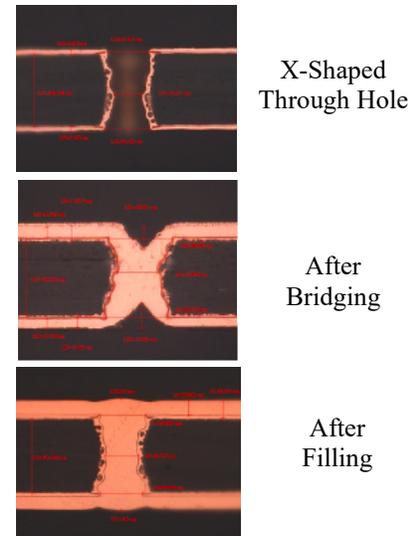


Figure 6. Stages of DC Copper Filling

The use of a single copper plating solution in a single step using DC chemistry is typically viewed as the “ideal” process for filling through holes with copper as it minimizes the number of plating tanks and shortens the overall dimensions of the physical plating line.

DC copper plating for through hole filling, however, is limited by the thickness of the substrate. For thin core materials of approximately 100um in thickness with through holes of 100um diameter at the outsides and 50-70um at the center, DC plating can be acceptable for filling the through hole with a plated surface copper thickness of less than 25um expected. As substrate thicknesses approach 200um, the propensity for the formation of cavities and inclusions increases as well as the necessity to plate much higher thicknesses of surface copper. This is due to the greatly extended plating times necessary to completely fill the through hole. Plating times of greater than 15-18 hours can be required to fill a through hole in a thick substrate utilizing DC plating chemistries. This effect is exacerbated for boards with mechanically drilled, straight walled, through holes as the “dogboning” tendencies of electroplating will tend to close the openings of the through holes more quickly (See Figure 7).

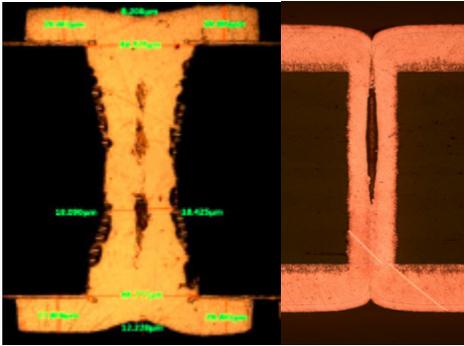


Figure 7. Cavity Defects and High Surface Copper in Thicker Substrates

BACKGROUND

Two Step Through Hole Fill Technology

In the two step through hole fill process, the bridging and filling steps are split into two separate steps utilizing two different plating solutions. The advantage of this methodology is that each process can be optimized for its intended function. The combined process offers a much more robust and flexible bridge and fill system capable of filling a broader range of hole diameters and substrate thicknesses with copper while minimizing excessive plated surface copper.

In the case of printed circuit boards, the two step through hole fill technology begins with either mechanically or laser drilled through holes processed through primary metallization including plasma and/or permanganate desmear and made conductive either through electroless copper or the commonly available direct metallization processes such as graphite, carbon black, or conductive organic polymers. A flash plate of copper can then be used to ensure conductivity across the entire through hole wall.

In the case of ceramic substrates, the through holes are typically laser drilled and made conductive by either electroless copper plating or sputtering a thin copper layer.

The bridging of the center of the hole to form a double via utilizes a periodic pulse reverse copper plating system optimized to provide a cavity-free bridge with minimal surface copper. The filling of the resulting double vias utilizes via fill copper plating technology to provide accelerated filling of the vias while also minimizing surface copper.

Bridge Step using PPR Plating

PPR plating is widely used for the conformal plating of high aspect ratio through holes. New rectifier designs and software now offer greater flexibility in developing complex waveforms that can provide plating results previously unobtainable. One of the features of newer rectifiers is the ability to impress asynchronous waveforms to each side of a

plating panel. An asynchronous waveform is a waveform that is impressed to each side of a panel but is offset a certain number of degrees greater than zero (See Figure 8).

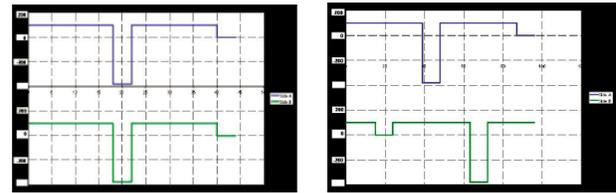


Figure 8. Example of Synchronous and Asynchronous Waveforms

The use of asynchronous pulsed waveforms can accelerate the plating rate of the copper in the middle of the through hole up to 5 times that of conventional pulse waves (See Figure 9).

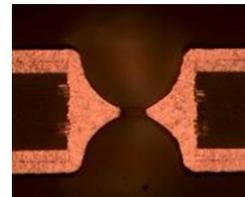


Figure 9. Example of Accelerated Plating at Hole Center

The electrolyte components of the bridge solution are typical of acid copper plating solutions: copper sulfate, sulfuric acid, chloride ion, and additives. The concentrations in this study are presented in Table 1.

Table 1. Bridge Bath Composition

Component	Concentration
Copper Sulfate	240g/L
Sulfuric Acid	110g/L
Chloride Ion	85ppm
Wetter	3%v/v
Brightener	0.05%v/v

Filling Step using Via Fill Plating

Copper via filling technologies have been widely used in the manufacturing of HDI and IC packaging substrates. Copper via fill baths are DC plating systems that are specifically designed for filling vias. They provide preferential copper deposition within the via and inhibited deposition on the substrate surface (See Figure 10).

This effect is accomplished by taking advantage of the difference in behavior of the additives in a via fill bath under different current density environments. The inside of the via is considered a low current density area versus the surface of the substrate. Suppressor additives in the via fill chemistry, in conjunction with chloride ions, adsorb onto and inhibit copper deposition in high current density areas. The brightener additives adsorb onto and accelerate copper deposition in low current density areas.

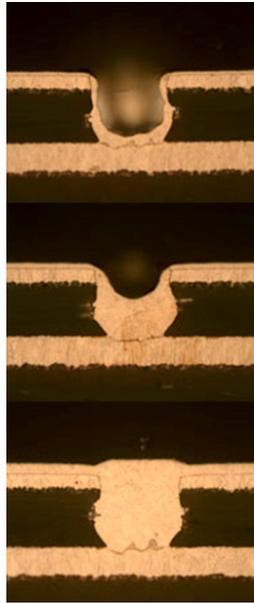


Figure 10. Example of Accelerated Plating within Via

At the beginning of the via fill process where the current density differences between the bottom of the via and top are the greatest, the differential in deposition rate is greatest resulting in bottom up filling. As the via fills, this differential in deposition rate decreases until the via is near filled at which point the deposition rates in the via and on the general surface become equal due to the equalization of current densities and adsorption of the various additives. At this point, the copper deposits at an equal rate on both the surface and in the via.

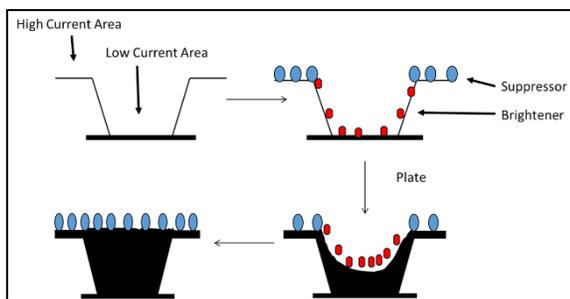


Figure 11. Mechanism of Via Filling

The electrolyte components of the via fill solution are typical of acid copper plating solutions: copper sulfate, sulfuric acid, chloride ion, and additives. The concentrations in this study are presented in Table 2.

Table 2. Via Fill Bath Composition

Component	Concentration
Copper Sulfate	200g/L
Sulfuric Acid	100g/L
Chloride Ion	75ppm
Wetter	0.9%v/v
Brightener	0.45%v/v
Leveller	0.8%v/v

EXPERIMENTAL

One of the key steps in the through hole bridge and fill process is the determination of the bridge cycle to form a via with a shape and dimensions that are optimal for filling. Generally, a via of approximately 7 mils or less in diameter with an aspect ratio of approximately 0.75 – 1.0 is preferred for optimal filling. In this paper, an experiment was run to demonstrate the behavior of the copper bridge as it develops. A DoE was also conducted to evaluate factors contributing to the characteristics of the bridging process. These factors included: Pulse Cycle, Current Density, Plating Time, Panel Thickness, and Hole Size. Experiments were also conducted to investigate the influences of the resulting bridge on further via filling.

RESULTS

Bridge Development and Optimization

The results of the bridging cycle testing with respect to time are summarized in Figure 12.

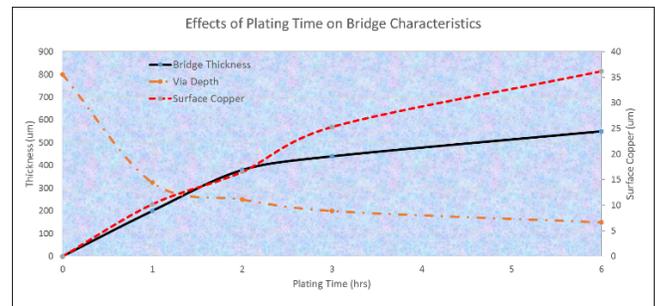


Figure 12. Bridge Characteristics vs Plating Time

The results showed that the bridge thickness increased quickly and linearly during the early stages of the process where the copper deposit extends outward from the center of the hole to close it and then begins to thicken and grow towards either side of the substrate surface. At a certain point, the rate of thickness increase of the bridge leveled out, with bridge thickness increasing only slightly thereafter with time. The via depth decreased greatly in the early stages of plating and leveled out at a certain point. This occurred in the region where the bridge thickness also leveled out indicating that little further change in via dimensions can be expected after this point.

The plated surface copper increased steadily during the entire process. Minimization of plated surface copper from the

bridge step is dependent upon the total plating time necessary to form an optimum via.

The change in the aspect ratio of the vias formed on either side of the plated copper bridge are presented in Figure 13.

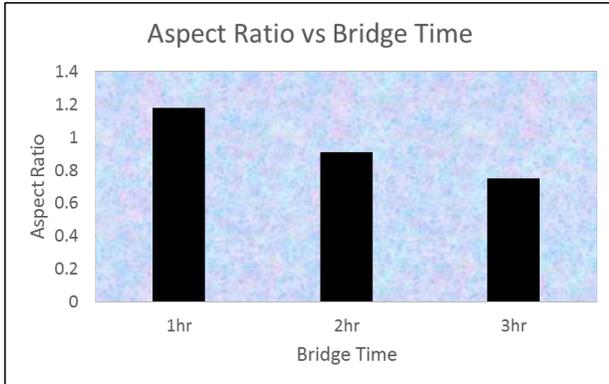


Figure 13. Via Aspect Ratio vs Plating Time

The results showed that the aspect ratio of the vias formed on either side of the bridge decreased with time. In this case, the desired aspect ratio of 0.75 was obtained in 3 hours for this particular hole size and substrate thickness. If the aspect ratio of the vias is too great, there will be a tendency to form cavities in the fill process as the tops of holes will close faster than the via can fill (See Figure 14). If the aspect ratios of the vias are too low or the diameters of the vias are too great, one will then get conformal plating due to the mechanism of differential current densities previously discussed.

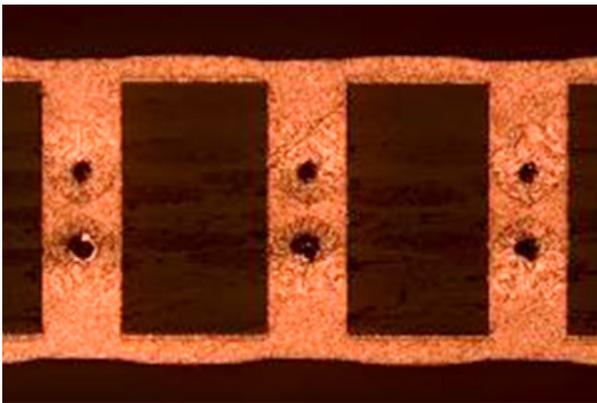


Figure 14. Cavities in High Aspect Ratio Vias

The main effects of the various factors investigated in the DoE on the resulting bridge thickness are presented in Figure 15.

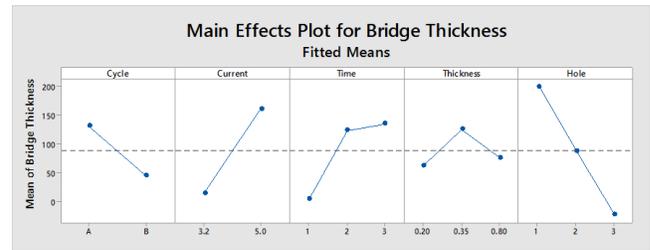


Figure 15. Main Effects on Bridge Thickness

The pulse cycle plays a great role in developing the bridge thickness by moderating the speed of accelerated deposition within the through hole. Increased current density also aids in bridge formation and thickness development by increasing the overall rate of copper deposition. Increased plating time allows the bridge to develop and grow. Increasing hole diameter has a negative effect on bridge thickness making it more difficult and time consuming to form and grow the bridge. Panel thickness had no significant effect on the bridge thickness.

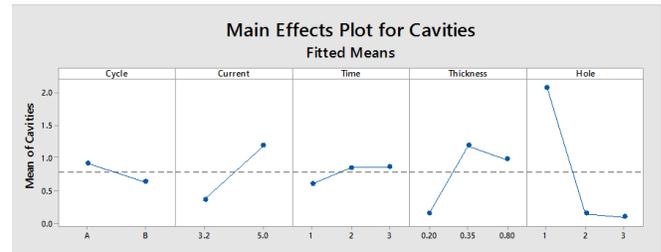


Figure 16. Main Effects on Cavity Formation

Factors having the greatest influence on the formation of cavities within the bridge in the through hole included current density, panel thickness, and hole diameter (See Figure 16). For a certain size hole, lower current densities allow for a slower, more controlled plating of copper to develop a dense, cavity free copper deposit. High panel thickness and small hole diameter can result in bridge formation from multiple points within the hole wall causing the formation of cavities (See Figure 17). Plating cycle and time had no significant effects.

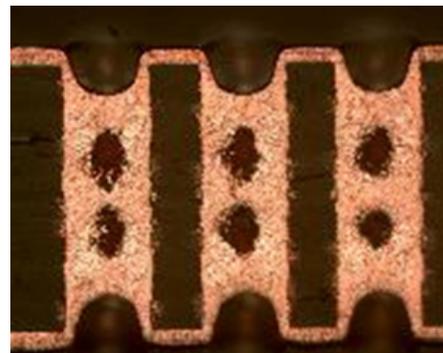


Figure 17. Effects of High Panel Thickness and Small Hole Diameter on Cavities

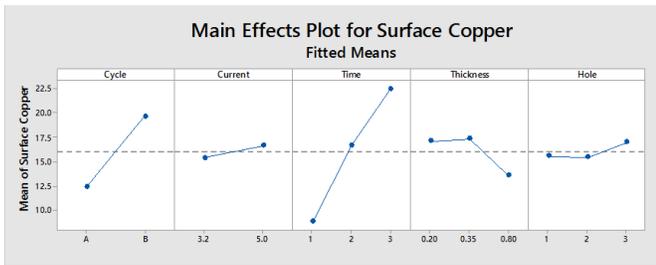


Figure 18. Main Effects on Surface Copper

The principal factors influencing the amount of surface copper plated onto a panel in the bridge process are the pulse waveform which controls the overall net forward current during plating and the total plating time. Current density, panel thickness, and hole diameter have no effect on the resulting surface copper thickness.

Effects of Hole Size and Substrate Thickness on Subsequent Via Fill Results

The data of total plated surface copper as a function of through hole diameter and panel thickness is presented in Table 3. The main effects plots are presented in Figure 19. The total plated surface copper is the sum of the plating thickness from both the bridge and the via fill processes.

Table 3. Total Surface Copper vs Hole and Panel Dimensions

Hole Dia	Panel Thickness						
	0.2mm 8mil	0.25mm 10mil	0.3mm 12mil	0.35mm 14mil	0.4mm 16mil	0.45mm 18mil	0.8mm 32mil
0.1mm 4mil	20um	22um	24um	26um	28um		
0.15mm 6mil	25um	27um	30um	33um	36um	40um	
0.2mm 8mil	30um	32um	36um	40um	44um	48um	75um
0.25mm 10mil	35um	37um	42um	46um	50um	56um	90um
0.3mm 12mil	40um	44um	50um	56um	60um	70um	110um
0.35mm 14mil	45um	50um	58um	65um	72um	80um	130um
0.4mm 16mil		55um	70um	85um	100um		
0.45mm 18mil							

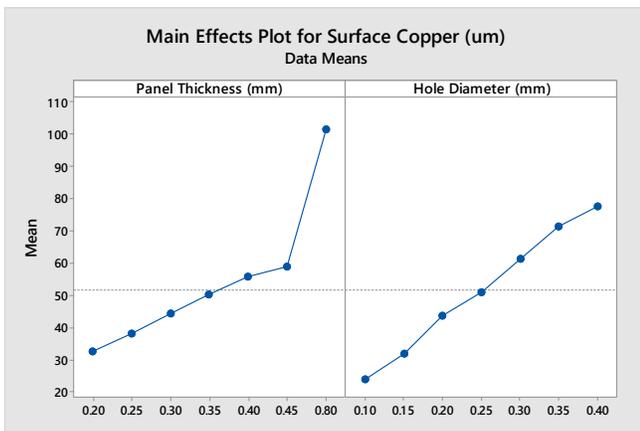


Figure 19. Main Effects Plot for Surface Copper

It is readily observed that hole diameter greatly affects the amount of total plated surface copper that can be expected for the through hole copper filling process. As the diameter of the through hole increases, the amount of surface copper that can be expected as a consequence of successfully meeting through hole filling requirements, increases. This is due to the fact that larger diameter holes require longer periods of time for the copper bridging process to extend across the diameter of the hole to close and form the vias and the longer periods of time to fully fill the resulting larger diameter vias. This can be substantial in the case of extremely wide holes.

It is also readily apparent that panel thickness greatly affects the amount of total surface copper for similar reasons. In the case of thicker panels, it requires more time for the bridge to build enough to provide vias of optimum aspect ratio. It logically follows that combining both large diameter holes with thicker substrates will result in more total plated surface copper than a thinner substrate with smaller diameter holes. This is illustrated in Figure 20. Plated surface copper for the thinner core material was 35um while the thicker core material was 93um.

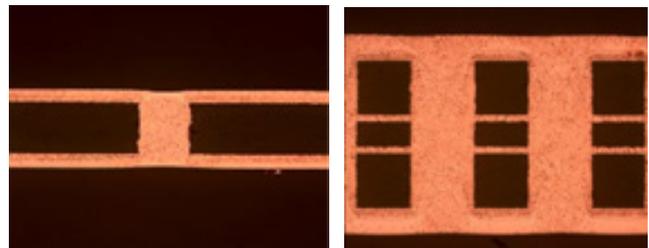


Figure 20. Effect of Substrate Thickness on Surface Copper

Another important characteristic of the copper plated through holes is the dimple size, especially if vias will be stacked or planarization is not desired. Large dimples can affect subsequent laser drilling processes when building additional layers resulting in poor product performance or failure. When flat surfaces are required, the presence of large dimples makes it necessary to build high thicknesses of plated copper so that the bottom of the plating vias is above the surface of the board. Planarizing can then be performed to make the copper plated through hole flush with the panel surface. This is typically undesirable as extra processes and costs are introduced into the manufacturing process.

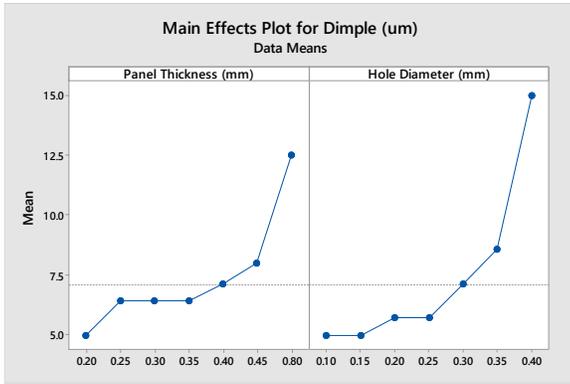


Figure 21. Main Effects Plot for Dimple Size

Figure 21 illustrates the main effects plots of hole diameter and panel thickness on dimple size. Dimple size, as with total copper surface plating, is greatly influenced by hole diameter and panel thickness. For a certain surface copper thickness, dimple size increases greatly with holes greater than approximately 0.25mm in diameter and with panel thicknesses of greater than approximately 0.4mm in thickness. The increase in dimple size with hole diameter is due to the geometry of the vias formed in these larger holes after bridging. The larger diameter, lower aspect ratio holes will have more of a tendency to conformal plate due to the mechanisms of via fill previously discussed (See Figure 22).

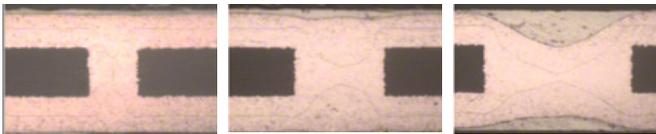


Figure 22. Effect of Hole Diameter on Dimple Size

The increase in dimple size with panel thickness is due to the greater time in forming the bridge and getting an acceptable via while controlling the plated surface copper within reasonable limits. The dimple can be reduced, but would require much more surface copper that might be objectionable to the manufacturer. Figure 23 illustrates this effect on 0.35mm holes in 0.25, 0.40, and 0.80mm core materials where plating was stopped as the maximum allowed plated surface copper was reached.

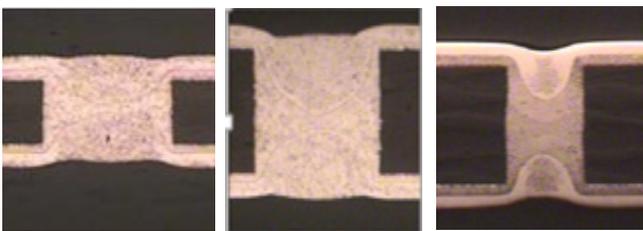


Figure 23. Effect of Panel Thickness on Dimple Size (0.25, 0.40, and 0.80mm core)

Limited work was done on the effect of the pitch of an array of holes on copper through hole filling in terms of dimple size. The results are summarized in Figure 24.

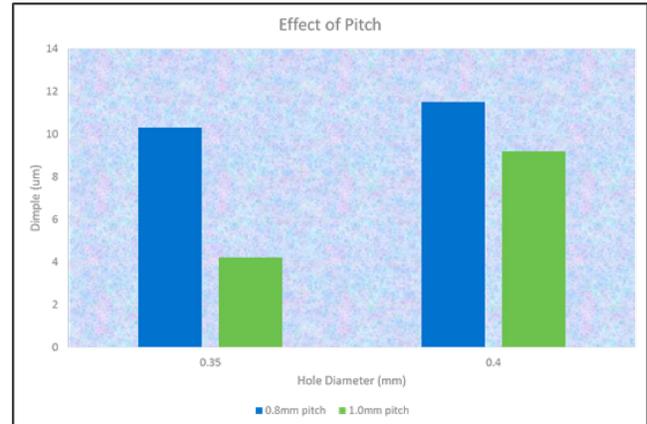


Figure 24. Effect of Hole Pitch on Dimple Size

The results indicated that, for a set hole diameter and panel thickness, the lower the pitch of the through holes (higher hole density), the larger the resulting dimple size. The reason for this phenomenon is that high density arrays can be considered high surface area features. As such, they will act as lower current density areas requiring longer times and/or higher current densities to meet minimum requirements versus isolated areas.

The physical properties of copper deposited in the copper through hole fill process are critical to the overall reliability of the electronic device in which it is used. Typical properties for the combined deposit are presented in Table 4.

Table 4. Typical Properties of Copper Through Hole Fill Deposit

Plating cycle	Sample #	Plated copper Thickness (mil)	Break Force (lbf)	Weight (g)	Elongation (%)	Tensile Strength (PSI)
Copper plated with bridging plus via fill process	1	2.82	62.75	0.9726	21.92	47098.0
	2	3.23	72.83	1.1146	21.19	47699.5
	3	2.71	60.21	0.9348	20.79	47018.9
	4	2.87	62.89	0.9901	19.46	46368.8
	5	3.05	68.12	1.0510	22.47	47314.6
	Mean	3.94	65.36	1.0126	21.17	47100.0

CONCLUSIONS

As technological advances continue in the electronics industry in the manufacturing of substrates for applications in HDI, IC, and LED, new challenges will arise for the design engineers. With continued trends toward miniaturization, new manufacturing techniques such as stacking of vias, and the use of high power devices that generate considerable heat, the need for improved methods of thermal management are required to efficiently conduct heat away from the electronic devices to improve device reliability and life. Copper through hole plating provides another tool to the engineer for the design of electronic circuitry. Figure 25 illustrates a real world application of copper through hole plating to conduct heat away from an LED device allowing it to operate at a lower temperature. In this example, the use of copper through

hole filling reduced the operating temperature of the device from 126C to 92C.

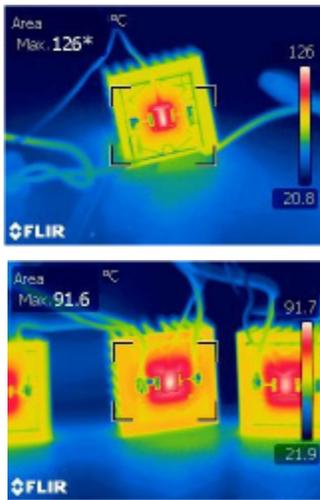


Figure 25. Use of Copper Through Hole Plating to Conduct Heat (Bottom Photograph)

The copper through hole plating process provides a versatile two step process consisting of a periodic pulse reverse step with specialized waveforms that allow the middle of a through hole to be bridged and sealed, forming two microvias that are subsequently filled with DC based via fill chemistries. The result is a highly reliable, highly thermally conductive copper filled via for the effective removal and dissipation of harmful heat from sensitive electronic devices.

The design engineer must understand the nuances of the copper through hole plating process and how the design of the board influences the results of each step of the plating

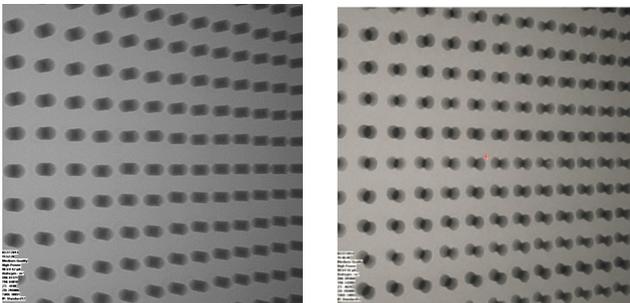


Figure 26. X-ray Imaging of Copper Through Hole Plating

process. The results presented in this paper illustrate the influence that board design features such as hole size and pitch and core thickness have on the critical outputs of the plating process such as ability to bridge, total plated surface copper, dimple size, aspect ratio, and total process time. When designing a substrate for the utilization of copper through hole plating, the design engineer must choose a

suitable substrate and thickness and incorporate hole sizes and layouts that will minimize output variations. In this way, a robust, reliable copper through hole process can be realized (See Figure 26).

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