Systek ETS 1200

Pattern Plating Metallization for Embedded Trace Substrates

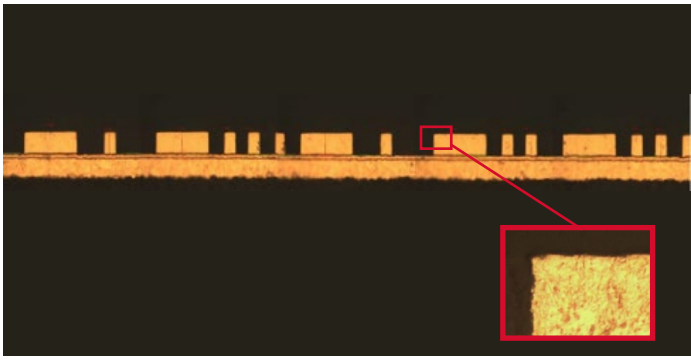
Pattern Plated Perfection, Embedded.

Systek ETS 1200 is an advanced DC acid copper pattern plating process specifically formulated for the construction of embedded trace substrates.

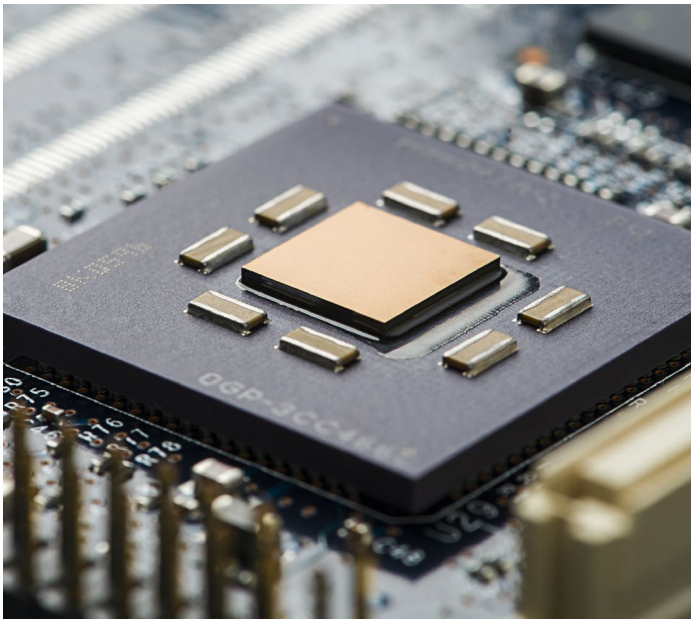
As the dimensions utilized in panel-level packaging have become finer and with extreme coplanarity requirements, embedded trace substrate technologies are being utilized to create the copper interconnections between the IC substrate and the silicon die.

The system plates copper traces down 5/5 µm line/space with very high coplanarity across pads and traces while delivering exceptionally flat trace profiles. These characteristics enable high reliability copper structures to be encased within laminate material for the ultimate in low impedance signal isolation.

The technology of the Systek ETS 1200 can be combined with the Systek Semi-Additive Processing and Systek UVF 2 in 1 plating technologies to create the most advanced IC substrate designs of today.



Systek ETS outerlayer (Inset: square trace profile and coplanarity detailed)



KEY FEATURES

- Fine line pattern plating down to 5/5 µm line/space
- High coplanarity of traces and pads for reliable connections to IC die with R-Values typically <2µm
- Excellent trace profile for controlled impedance
- Low-stress deposit exceeds IPC Class III standards for tensile and elongation (6012D, DS, DA, 6013D)
- Fully analyzable 3-component system for high degree of process control

MacDermid Enthone

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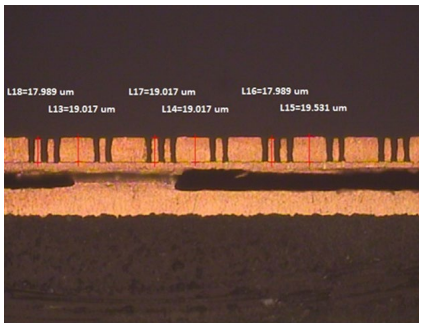
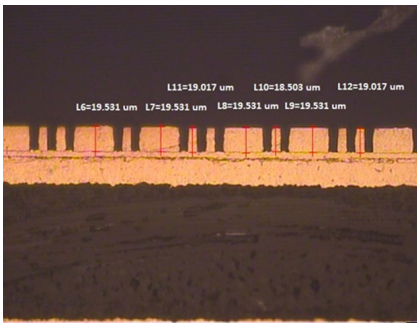
Embedded Trace Substrates Enable High Performance Designs

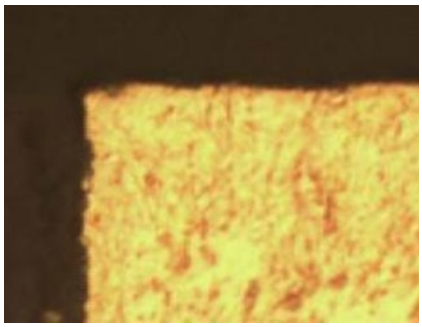
Systek ETS is a panel-level packaging solution that enables very high density outerlayers on organic IC substrates. The process is production-proven for designs of 7 micron lines and spaces, and is ready to accommodate further increases in circuit density. The square profile of the embedded traces maintains electrical signal integrity with very low impedance, improving layer performance.



5/5 µm L/S on Carrier

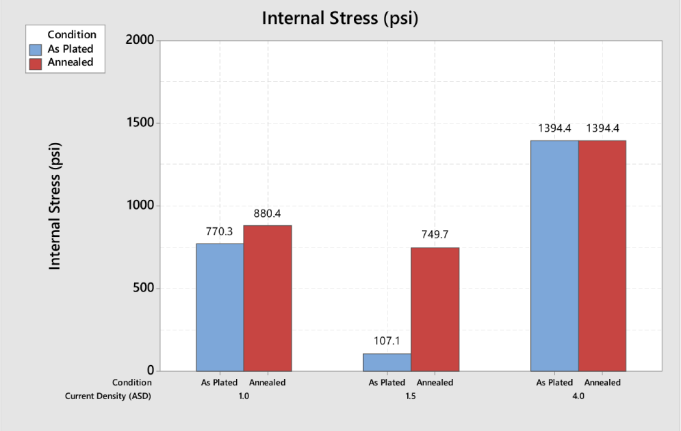


7/7 µm L/S on Carrier



Square Trace Profile

Excellent Deposit Properties and Plating Performance



Systek ETS 1200 plates a copper deposit with very low internal stress across a wide current density range, ensuring that the deposit does not contribute to warpage of the substrate.

Coplanarity, WIU Compared to Pad (50 µm)		
Line/Space (µm)	R-Value Max (µm)	R-Value Average (µm)
10/10	0.29	0.11
7/7	1.03	0.68
5/5	1.54	0.86

Systek ETS 1200 panel plates fine traces and pads onto a copper carrier with R-Values across individual units and entire panels consistently below 2 µm, for excellent manufacturing quality and build-up compatibility.

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