

Optimizing Morphology of Plated Copper Sub Assemblies through Oxide Alternative Process

John A. Marshall
MacDermid Inc.
245 Freight Street
Waterbury, CT 06792

Topic Number T5.1 Chemical Technology - Oral Presentation

Abstract

This paper discusses the investigation and testing to better understand the effect of baking plated copper sub-assemblies before Oxide Alternative process.

Previous documented work had discussed the benefits of baking electroplated copper before Sulfuric acid and Hydrogen Peroxide type micro-etches including "Oxide Alternatives". This paper focuses on achieving consistent etch rates and improving the consistency and uniformity of the resulting copper surface morphology by baking electroplated copper sub-assemblies to anneal the copper before Oxide Alternative Process.

We have seen that different types of electroplated copper and plating conditions react differently when measuring etch rates with various hold times at room temperature after plate and also with baking after plating. Etch rates were measured and compared using standard weight loss coupons and plated copper coupons. Copper surface roughness was measured using Zygo Light Interferometer.

Synopsis

With the prevalence of HDI printed circuit boards utilizing electrolytic plated acid copper sub-assemblies with faster signal speed, we have seen an increasing concern over uniform, consistent copper surface morphology following inner layer bonding promotion treatment utilizing an "Oxide Alternative" micro-etch process. Typically, these "Oxide Alternatives" are hydrogen peroxide and sulfuric acid based combined with organic additives to create a micro-etched roughened copper surface with an organo-metallic coating. The oxide alternative process optimizes both the mechanical and chemical bonding of the PCB inner layers by increasing copper surface bonding area with a cuprous rich organo-metallic coating, providing a thermal barrier between the prepreg resin and the copper surface.

Studies have detailed the research into the "Self Annealing" or "Re-crystallization" phenomenon of electroplated copper, occurring at room temperature as a micro-structural evolution process occurring at room temperature. There has been general agreement that grain growth is the primary mechanism for copper re-crystallization. There have been several studies showing the effect of electroplating process parameters, including organic and inorganic additive type(s), concentration(s), current density and copper film thickness on "Self Annealing" and the termination or re-crystallization. Diffusion/desorption of carbon containing molecules from the plating bath additives incorporated in the copper film were proposed as a mechanism for grain growth and stress release.^{1, 2}

Non-correlated behavior had been observed in monitoring of Sheet Resistance and Stress, indicating there are factors other than copper grain growth alone that may be involved in the re-crystallization at room temperature. Also proposed was the mechanism of the redistribution of trapped (co-deposited) organic additives, prior to the grain growth, acting as a trigger for the self-annealing. However, another study observed no significant spontaneous redistribution of the organic impurities when self-annealing did not occur, suggesting that any redistribution followed self-annealing and was not a significant trigger for self-annealing. Instead grain growth appeared to force the impurities to be redistributed.³

More recently, studies have discussed changes both in grain size and their orientation finding many high-angle grain boundaries before self-annealing. After self-annealing, the copper grains in the electroplated film were seen to have many multiple twins, coming from low stacking-fault energy of copper.⁴

While there is some disagreement of the actual sequence of plating additive diffusion and grain growth in self-annealing, there is agreement that the as-plated films are not stable, with their microstructure evolving at room temperature. However, at room temperature the re-crystallization is not "under control" and not uniformly consistent, depending on the electroplating process variables including additive type(s), concentration(s), current density and copper film thickness.

We had observed significant variation in the plated copper etch rates and surface morphology after oxide alternative process, depending on the actual electroplating chemistry conditions and hold time after plating. It became apparent that relying on copper self-annealing at room temperature was very time dependent and not entirely consistent. With reduced P.C.B. turnaround times, a 24 to 36 hour hold after plating before oxide alternative is not always practical. A paper published in 2003 detailed the relationship between the self annealing of plated copper and copper surface treatment utilizing sulfuric peroxide type chemistry. Also discussed was the effectiveness of anneal baking before sulfuric/peroxide roughening microetch (oxide alternative), to consistently terminate the copper re-

crystallization.⁵ PCB companies slowly started following the recommendation to “anneal bake” freshly plated copper for 15 minutes at 130°C before “Oxide Alternative” process. A significant improvement in overall uniformity of etch rate, oxide alternative coating and copper surface roughness was observed.

We had identified and confirmed the effectiveness of an “annealing” bake after plating before oxide alternative process in order to achieve a stable etch rate and consistent, uniform plated copper surface morphology without waiting for 24 to 36 hours (or longer) for the plated copper to re-crystallize. Plated test coupons were processed through 2 different oxide alternative oxide processes with no hold time after plating, bake for 60 minutes at 90°C directly after plating, 5 days hold time after plating and 5 days hold plus baking 60 minutes at 90°C. Etch rate and chemical conditions were maintained for all of the test coupons. Test results indicated that coupons processed through both oxide alternatives directly after copper plate were rougher and had increased surface roughness variation compared to standard ED foil. Baking plated copper resulted in reduced, consistent etch rates with reduced, uniform surface roughness. Baking directly after plating resulted in etch rates and surface roughness similar to a five day hold after plating, before oxide alternative. (Fig 1 & Fig 2)

Fig 1. Oxide Alternative A - Etch Rate Target of 55u"

	Ra - Microns	Ra Cv%	RSAR	RSAR Cv%
ED Cu Start	0.25	6.6	0.18	6.7
ED Cu after 55.7u"	0.49	4.1	0.45	4.5
Fresh Plate Start	0.38	4.8	0.15	5.7
Fresh Plate - 52.4u"	0.83	9.6	0.59	12.8
Fresh Plate + Bake - 42.6u"	0.75	5.8	0.45	1.9
5 days after Plate - 41.8u"	0.71	7.1	0.44	2.7
5 days after Plate + Bake - 39.4u"	0.74	6.4	0.47	2.1

Fig 2. Oxide Alternative B - Etch Rate Target of 75u"

	Ra - Microns	Ra Cv %	RSAR	RSAR Cv %
ED Cu Start	0.25	6.6	0.18	6.7
ED Cu after 74.3u"	0.59	9.9	0.51	8.5
Fresh Plate Start	0.38	4.8	0.15	5.7
Fresh Plate - 76.8u"	0.78	11.3	0.54	7.6
Fresh Plate + Bake - 57.8u"	0.62	4.8	0.39	2.9
5 days after Plate - 59.2u"	0.64	4.6	0.42	3.3
5 days after Plate + Bake - 63.4u"	0.6	4.4	0.4	3.1

A potentially serious reliability issue had been observed sporadically in plated copper sub-assemblies after oxide alternative, with deeply etched “spikes” or “tunneling” into the plated copper. These etched spikes were typically 5 microns up to 20 microns deep and in some cases extended all the way to the foil copper. However, these etched “spikes” did not continue down into the foil copper. (Fig 3 & 4)

Fig 3 – Etched “Spikes”

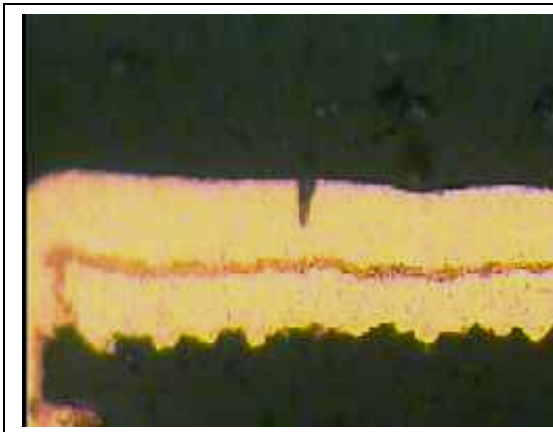
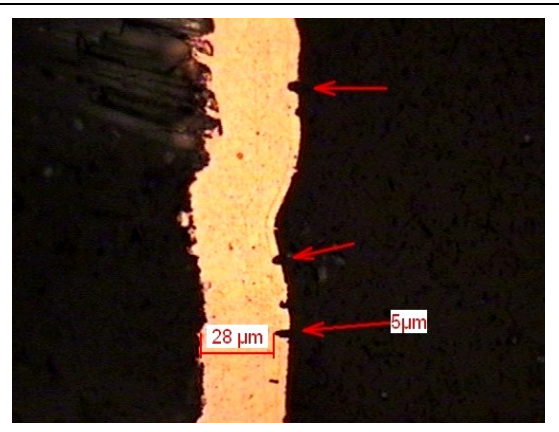


Fig 4 – Etched “Spikes”



After back-tracking through production logs and bath analysis records, the problem had been identified as having a direct correlation to instances of high levels of organic additives in electrolytic copper bath. Baking for one hour at 100°C after plating, before “oxide alternative”, was found to be effective in eliminating the etched “spikes” and improving the uniformity of the copper surface roughness.

Many of the newer copper baths used for via filling operate at higher additive levels, requiring a more aggressive annealing bake before oxide alternative in order to produce uniform copper etch rate and morphology.

Conclusions

Using an “annealing bake” of 1 to 2 hours at 90°C-120°C (200°F-250°F) before oxide alternative was found to be significantly more reliable than self annealing at room temperature and was considerably faster than waiting 24 to 36 hours for self annealing at room temperature. As a result of baking, we found that an “anneal bake” normalized both the etch rate and morphology of freshly plated copper.

Customer tests confirmed the effectiveness of an anneal bake in producing consistent etch rates and uniform copper surface morphology. Baking plated sub-assemblies before oxide alternative also proved to be very effective in eliminating deeply etched “spikes” that can result from excess organic additives in the electrolytic copper bath.

References

1. Impurity Redistribution in Electroplated films during Self Annealing.
Ming-Sueng Yoon Thin Solid Films, April 2002
2. Self-Annealing characterization of Electroplated Copper Films.
S. Lagrange, MicroElectronic Engineering, January 2000
3. Characterization of Electroplated Copper Self-Annealing with Investigations focused on Incorporated Impurities
M. Stangel, Leibniz Institute for Solid State and Materials Research, August 2005
4. The Effect of Plating Current Densities on Self Annealing Behaviors of Electroplated Copper Films.
Shih-Chieh Chang, Institute of Materials Science & Engineering, National Chia Tung University, Taiwan
5. The relationship between Self-Annealing of Plated Copper and copper surface treatment. T. Nakagawa, Circuit World Volume 29, 2003

Biography

- Applications Manager for the World Wide Circuit Formation Product Group at MacDermid Inc. Waterbury CT, USA.
- PCB industry veteran of 35+ years, working in PCB manufacturing, Chemical and Equipment sales and service.
- Introduced and commercialized the first Aqueous Liquid Photoimageable Soldermask in the USA, 1986
- Member of AES, Merrimack Valley chapter 1984 – 1987.
- Founding Member of North East Circuits Association, 1987. Technical Presenter and Program Chairman 1987 - 1998
- BA from Bowdoin College, Brunswick Maine, 1973